COMS3100/7100 Introduction to Communications

Lecture 23: ***Phase-Lock Loop (PLL)***

This lecture:

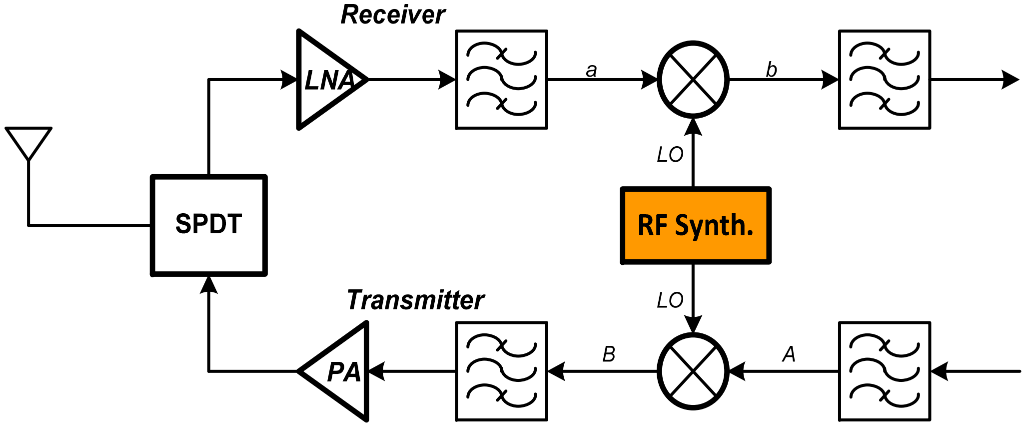
- PLL operation and lock-in
- Linearised PLL model and FM detection
- ***Frequency synthesizers***
- ***Synchronous detection***

Ref: ***Carlson***, Chapter 7.3; ***R. E. Best***, "Phase-Locked Loops: theory, design and applications" McGraw Hill, 1984; ***J. R. Smith***, "Modern Communication Circuits", McGraw Hill, 1998

Frequency Synthesizer

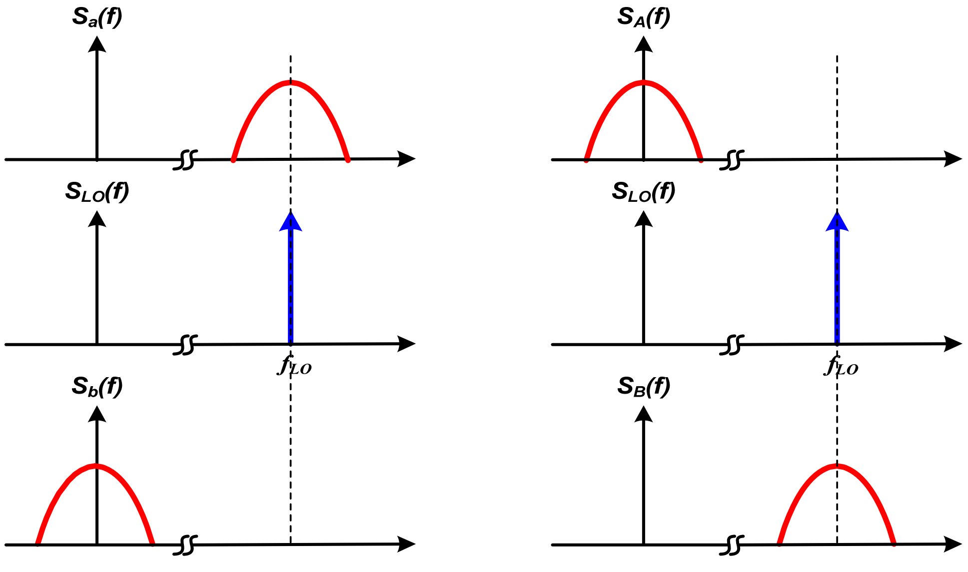
- Essential component in communication system for frequency translation

- Frequency synthesizer generates the LO signal



$$S_b(f) = S_a(f) * S_{LO}(f)$$

$$S_B(f) = S_A(f) * S_{LO}(f)$$

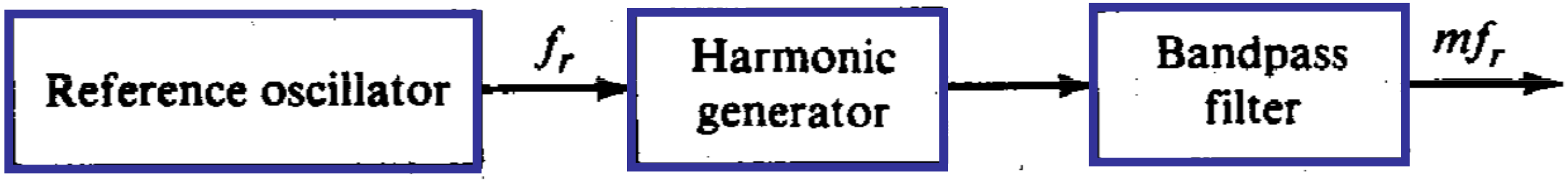


(a) Rx

(b) Tx

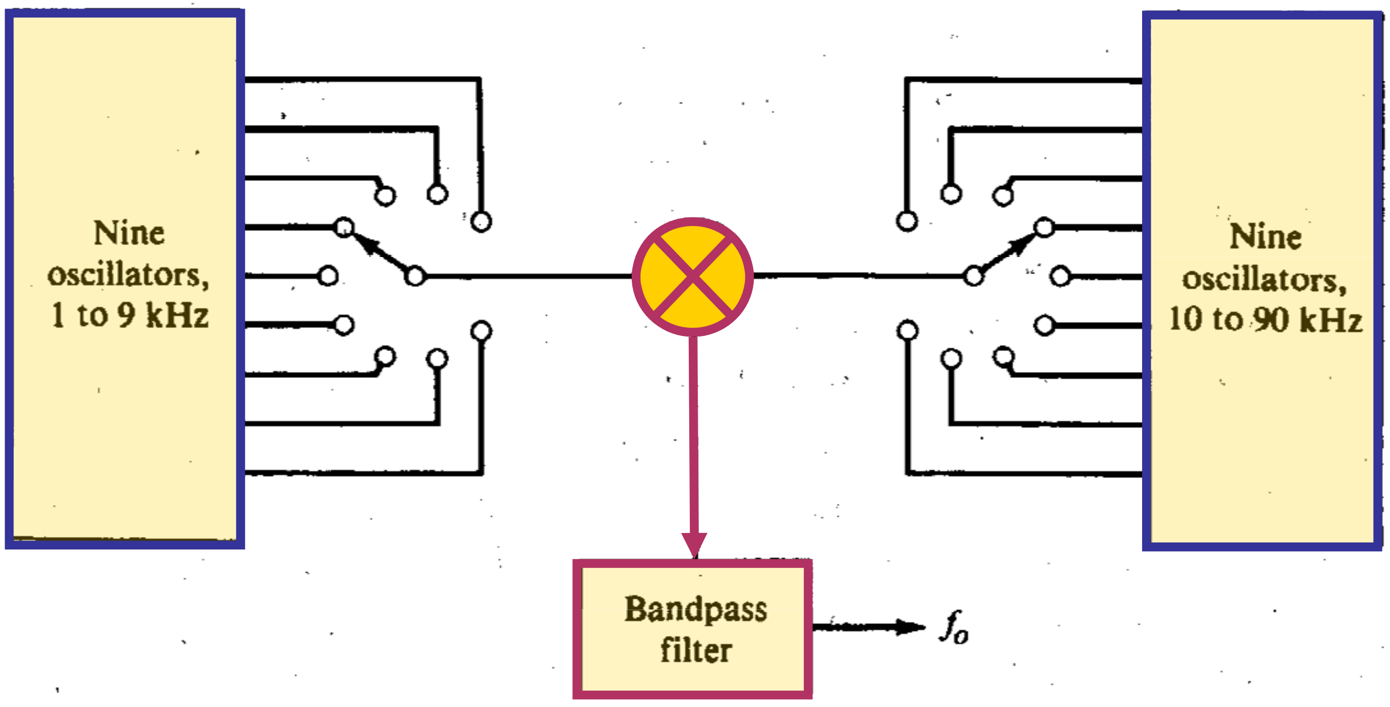
Direct Frequency Synthesis

- The oldest of the frequency synthesis methods.
- Direct frequency synthesis refers to the generation of few frequencies from one or more reference frequencies by using a combination of:
  - harmonic generators, filters, multipliers, dividers and mixers.
- All frequencies stabilised and synchronised to master oscillator
- One method is shown below.
  - The desired frequency is obtained with a filter tuned to a given output frequency.
  - Requires highly selective filters.



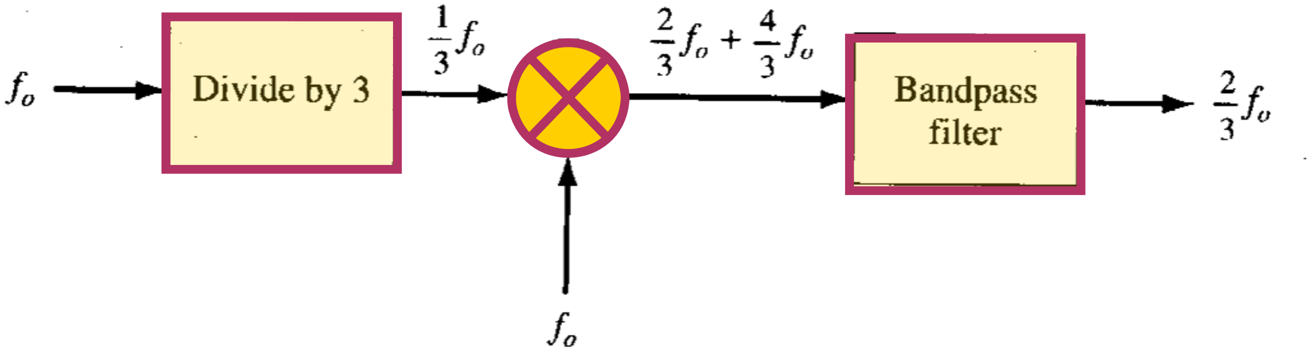
Direct Frequency Synthesis

- An alternative approach is to use multiple oscillators.
- Synthesizer shown below generates 99 frequencies from 18 oscillators;
- BPF selects the higher of the two mixed frequencies



Direct Frequency Synthesis

- Example of direct synthesis; the new frequency (2/3)f_0 is realised from f_0 by using a divide-by-3 circuit and a mixer and BPF.

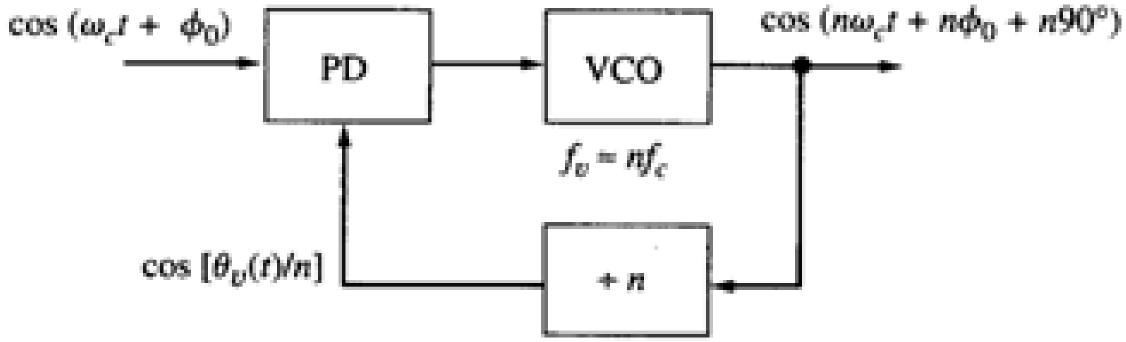


- One of the most critical considerations is the mixing ratio $r = f_1/f_2$
- If r is too large or too small frequencies are too close and hard to separate by filtering

- The problems associated with direct synthesis are greatly reduced with the frequency synthesis technique that employs a PLL

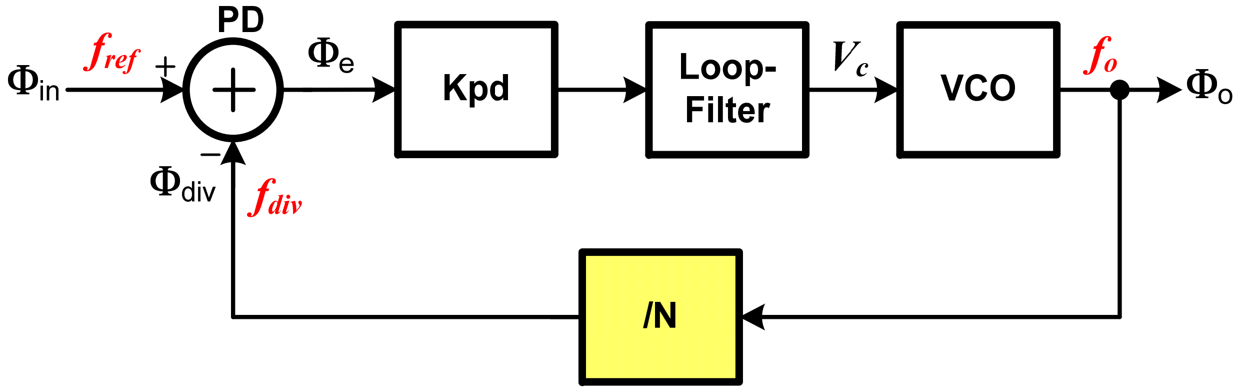
PLL Frequency Multiplier

- Feedback loop frequency is divided by n
- Loop gain is now effectively K/n
- Note $\div n$ implemented divide-by-n counter
  - Adjustable frequency multiplier
- LPF cut-off frequency must be reduced as *n* is increased



Frequency synthesis by Phase Lock

- Basic FS-PLL architecture

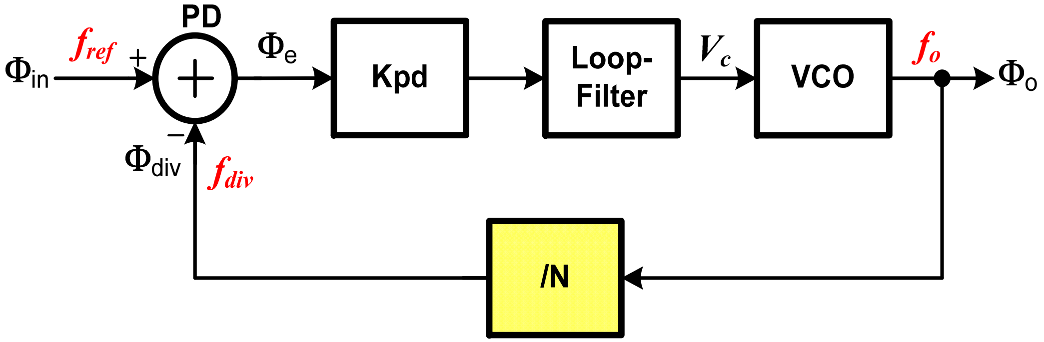


- What's PLL-based Frequency Synthesizer?
  - $f_o = N * f_{ref}$
  - f_{ref} : reference frequency, typically from a crystal oscillator (XO).
  - Sensitive to loop parameters (loop-gain, phase-margin, loop BW, etc) due to the negative feedback loop.
  - Loop gain proportional to 1/N

Frequency Synthesizer PLL

- Why use PLL as a frequency synthesizer?
  - As a local oscillator with a high accuracy and purity.
  - To translate the frequency accuracy of a high quality signal source to a tunable signal source.
  - To translate the noise characteristics of a high quality signal source to a lower quality signal source.
- Design Parameters :
  - Frequency accuracy
  - Phase noise (in-band / out-of-band)
  - Reference / Fractional spurs
  - Settling time (or Channel switching time / Lock-up time)
  - Input sensitivity
  - Power consumption
  - Size, cost, etc

Transfer function of the PLL based frequency synthesizer



$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{K_d K_o F(s)/s}{1 + K_d K_o F(s)/(Ns)} = \frac{G(s)}{1 + G(s)/N} \qquad (8.4)$$

The same transfer function relates the input and output frequencies $f_r(s)$ and $f_o(s)$.

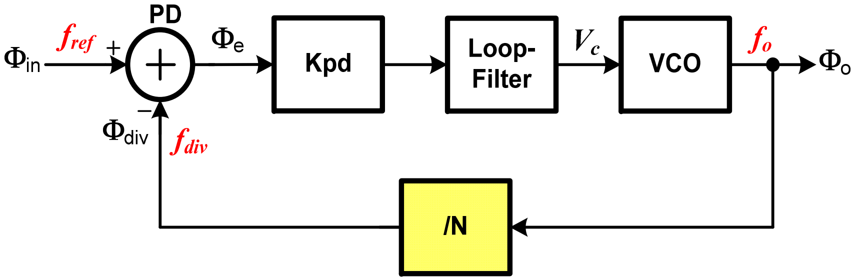
If no low-pass filter is used, the transfer function is

$$\frac{\theta_o}{\theta_r} = \frac{K_d K_o}{s + K_d K_o/N} = \frac{N K_v}{s + K_v}$$

which is equivalent to the transfer function of a simple low-pass filter with a dc gain of N and a bandwidth equal to K_v, where

$$K_v = \frac{K_d K_o}{N}$$

PLL based frequency synthesizer – an Example



A frequency synthesizer uses a PLL to synthesize a 1-MHz signal from a 25-kHz reference frequency. To realize an output frequency of 1 MHz, a division of

$$N = \frac{10^6}{25 \times 10^3} = 40$$

must be included in the feedback path. If no filtering is included, the closed-loop transfer function will be

$$\frac{\theta_o}{\theta_r} = \frac{K_d K_o / s}{1 + K_d K_o/(sN)} = \frac{K_d K_o}{s + K_d K_o/N}$$

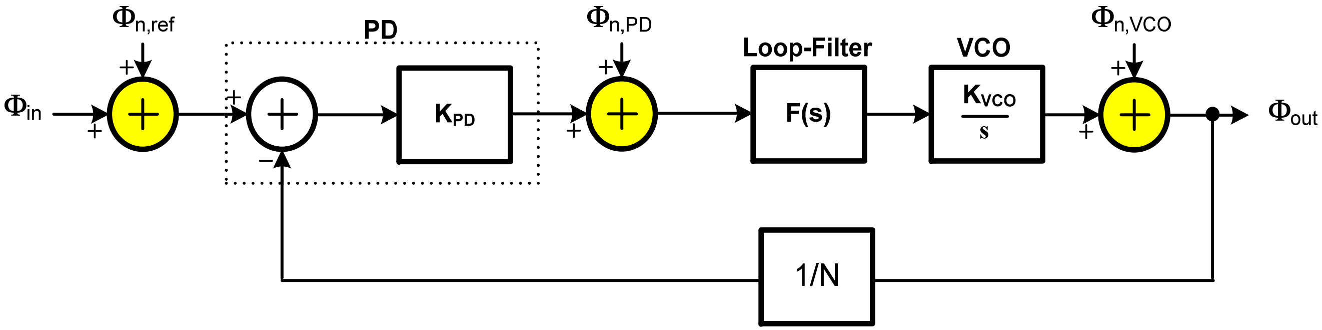
A typical value for K_d is 2 V/rad, and a typical value for the VCO gain factor K_o (for a 1-MHz VCO) is 100 Hz/V. With these values the closed-loop transfer function is

$$\frac{\theta_o}{\theta_r} = \frac{(2 \times 100)2\pi}{s + (2 \times 100 \times 2\pi)/40}$$

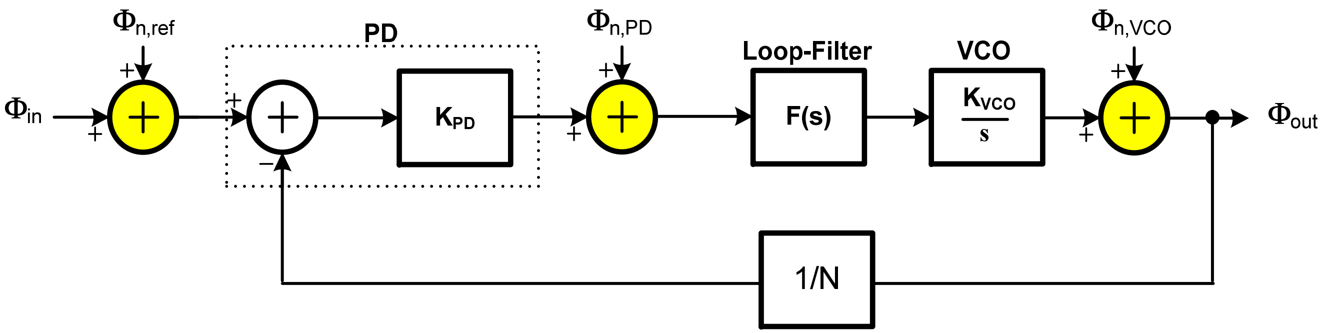
The synthesizer bandwidth will be $(2 \times 100)/40$, or 5 Hz.

Effect of Reference Frequency on Loop Performance

- To obtain fine frequency resolution, the reference frequency must be small. This also requires large N values, then causing large variations in the open-loop gain
- Secondly the loop bandwidth needs to be less than the reference frequency because the LPF must filter out the reference frequency and its harmonics present at the PD output.
- Finally the effect of noise introduced in the VCO becomes pronounced. Three main sources of noise are
  - Noise of the reference signal - $\Phi_{n,ref}$
  - Noise created by the phase detector - $\Phi_{n,PD}$
  - Noise introduced by the VCO – $\Phi_{n,VCO}$



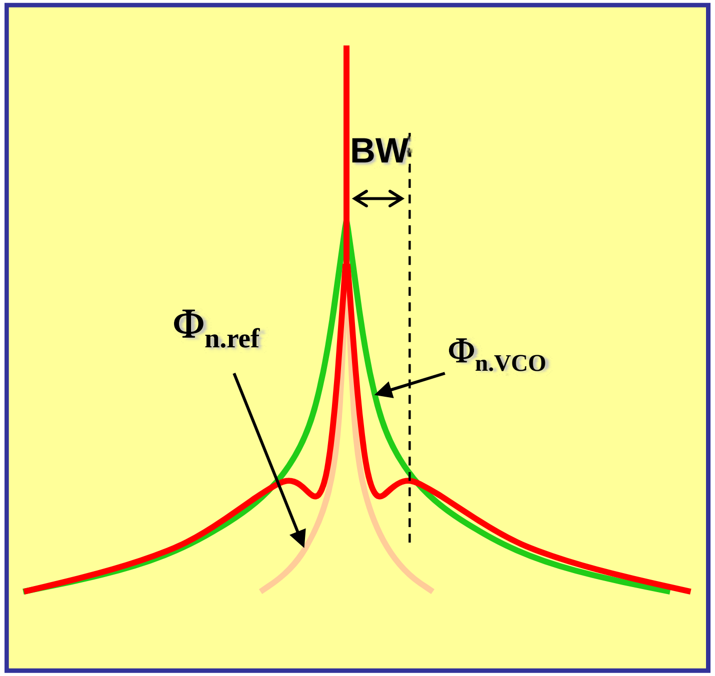
Noise Characteristics of the PLL synthesizer



$$\frac{\Phi_{\text{out}}}{\Phi_{\text{n,ref}}}=\frac{G(s)}{1+G(s)/N}=H(s)$$

$$\frac{\Phi_{\text{out}}}{\Phi_{\text{n,PD}}}=\frac{1}{K_{PD}}\cdot\frac{G(s)}{1+G(s)/N}=\frac{1}{K_{\text{PD}}}\cdot H(s)$$

$$\frac{\Phi_{\text{out}}}{\Phi_{\text{n,VCO}}}=\frac{1}{1+G(s)/N}$$



- PLL acts as a ***lowpass filter*** for the phase noise arising in the reference signal and the phase detector, and as a ***high-pass filter*** for the phase noise originating in the VCO

Phase Noise and Jitter in PLL synthesizers

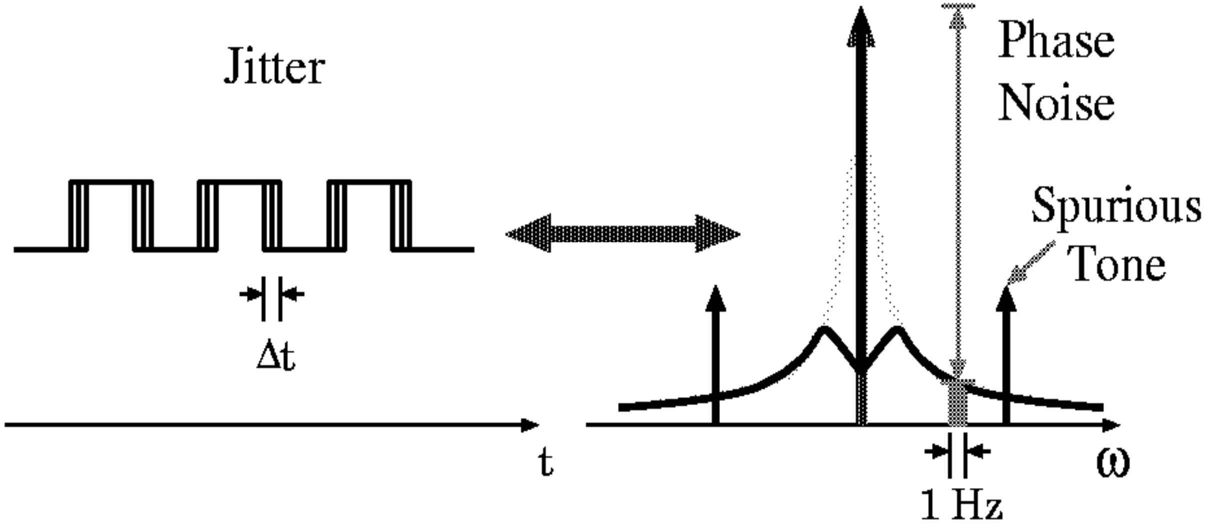
Time Domain ↔ Frequency Domain

Jitter ↔ Phase Noise

- Cycle-to-cycle Jitter
  : two consecutive pulses
- Peak-to-peak Jitter

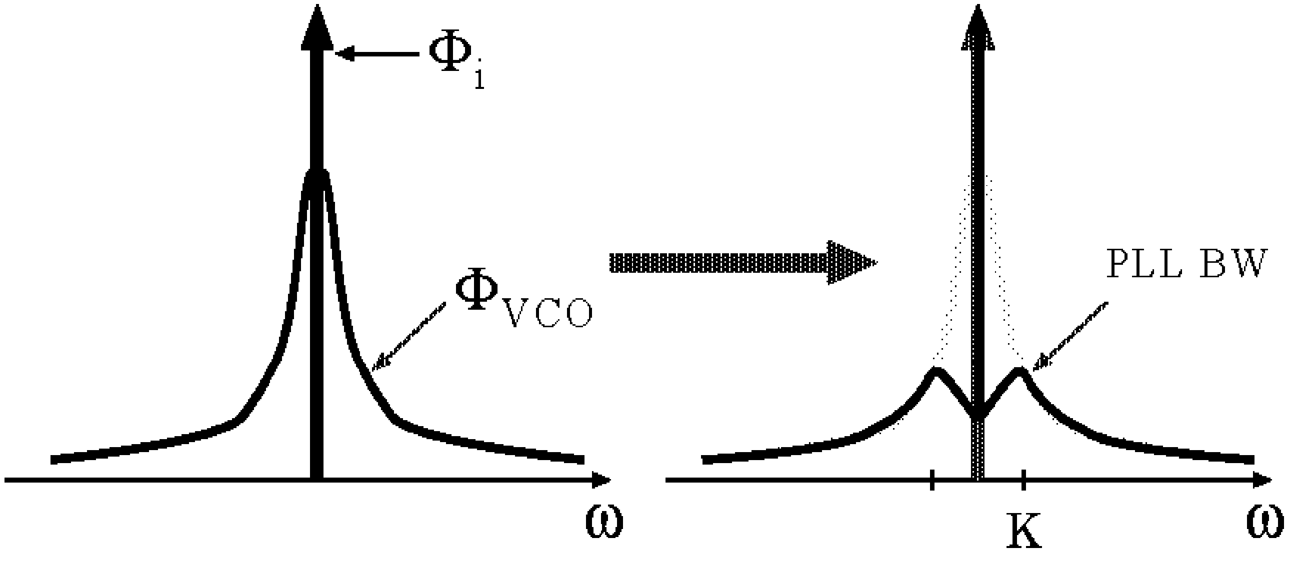
Spurious Tone

- From f_r



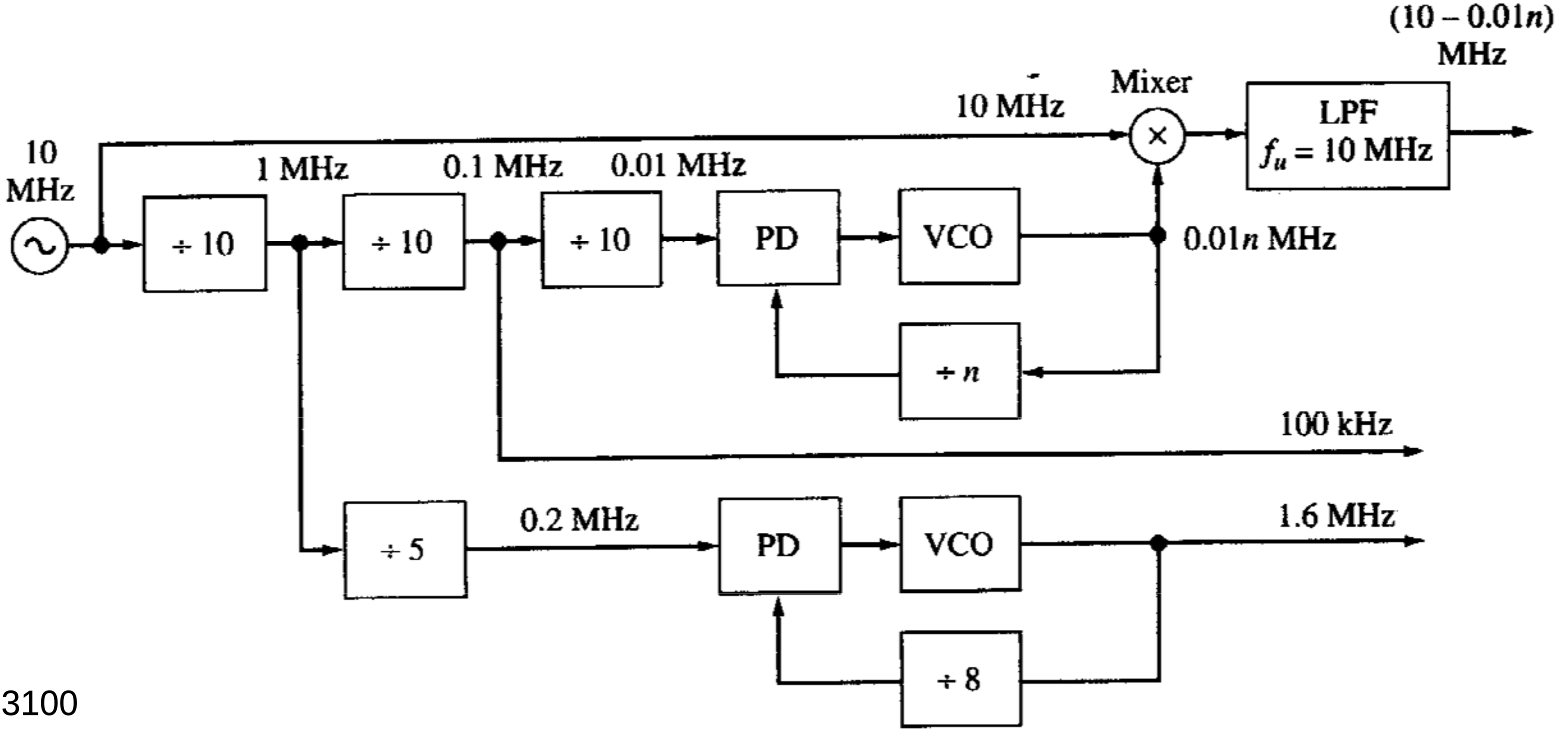
Frequency Domain Analysis (cont.)

- To reduce phase noise or jitter
  - VCO noise dominated system : Increase the loop bandwidth
  - Reference XO/PD noise dominated system : Decrease the loop bandwidth.



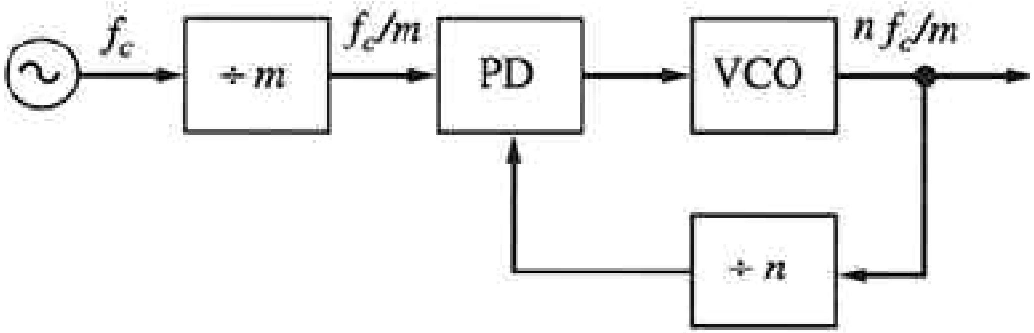
Example 1 (Carlson 7.3-1):
Frequency synthesizer with fixed and adjustable outputs

- Double conversion SSB receiver needs:
  - fixed LO at 100 kHz (for synchronous detection),
  - fixed LO at 1.6 MHz (for the second mixer) and
  - Adjustable LO from 9.9 to 9.99 MHz in 0.1 MHz steps (for RF tuning)
- From a single 10 MHz master-oscillator
  - Note: all output frequencies are less than master
    - Reduces **absolute** frequency drift (relative drift constant)



Example 2 (Carlson Exercise 7.3-2)

- Design a PLL system that synthesises nf_c/m from f_c master oscillator.



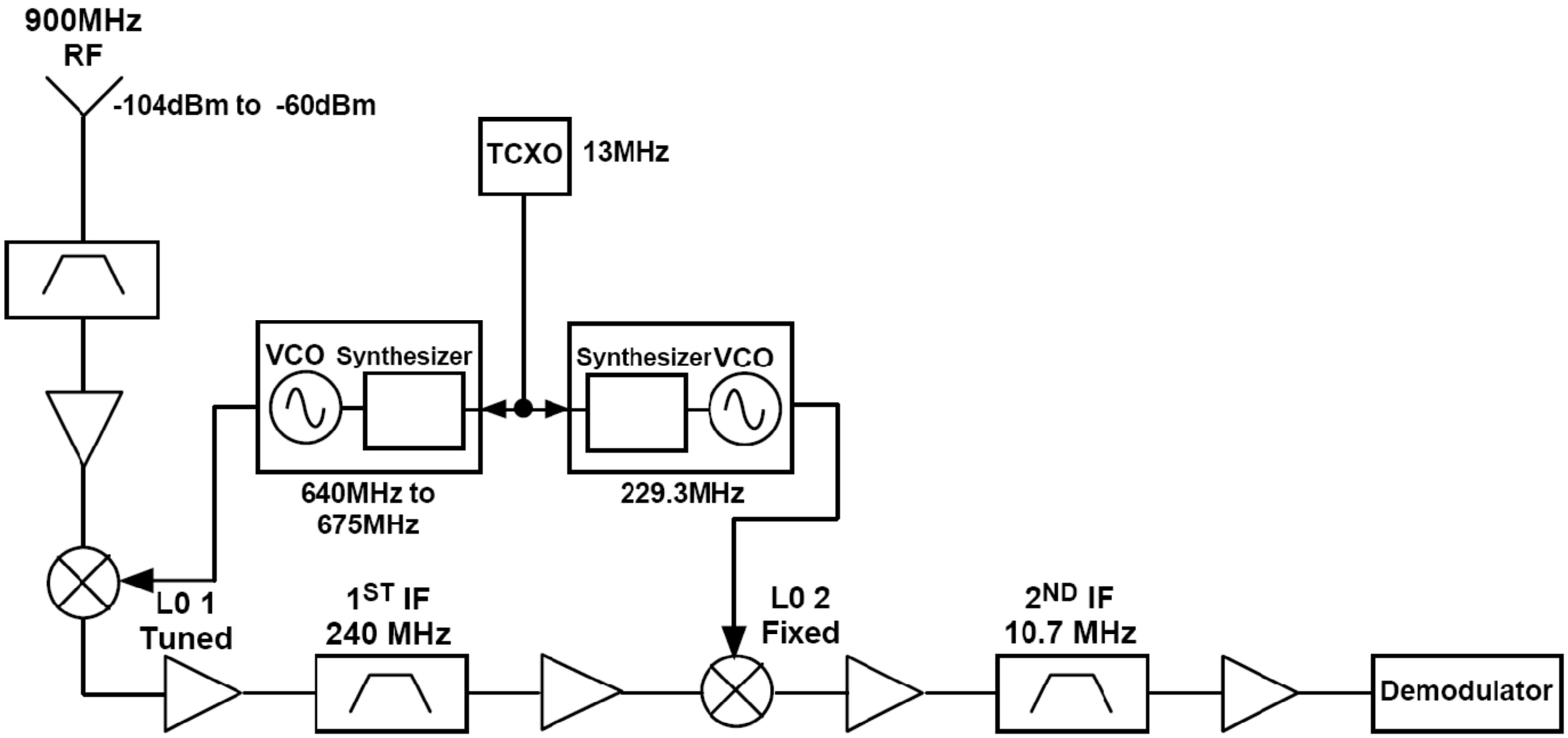
- VCO free run frequency and lock in condition on loop gain K

$$f_v = \frac{nf_c}{m} - \Delta f$$

$$K \geq |\Delta f| = \left| f_v - \frac{nf_c}{m} \right|$$

Example 3:Frequency synthesizer with fixed and adjustable outputs for the GSM base-station receiver

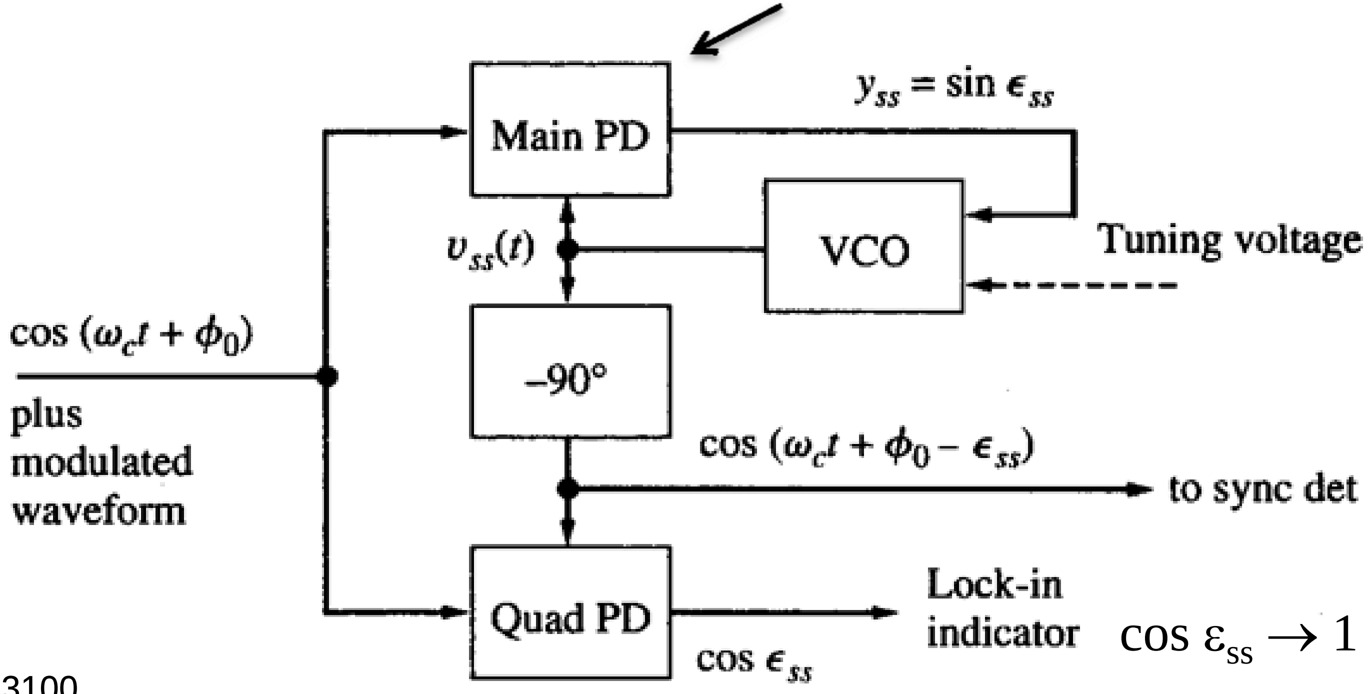
- In addition to the tunable RF LO, the receiver section also uses a fixed IF (in the example shown this is 240 MHz). Even though frequency tuning is not needed on this IF, the PLL technique is still used. The reason for this is that it is an affordable way of using the stable system reference frequency to produce the high frequency IF signal.



Synchronous Detection with pilot

- Important application for PLLs is
  - Synchronization of receiver local oscillator
- Beneficial to use pilot carrier for synchronous detection
  - PLL tracks phase and frequency drift in pilot
- Acts as ***narrowband pilot filter*** with very low noise
- Can also be used to search for signals – apply ramp to tuning I/P

PC + LPF + K



Brings VCO $\rightarrow f_c$

$\therefore \varepsilon_{ss} \approx 0$

i.e., to LO

$\cos \varepsilon_{ss} \rightarrow 1$

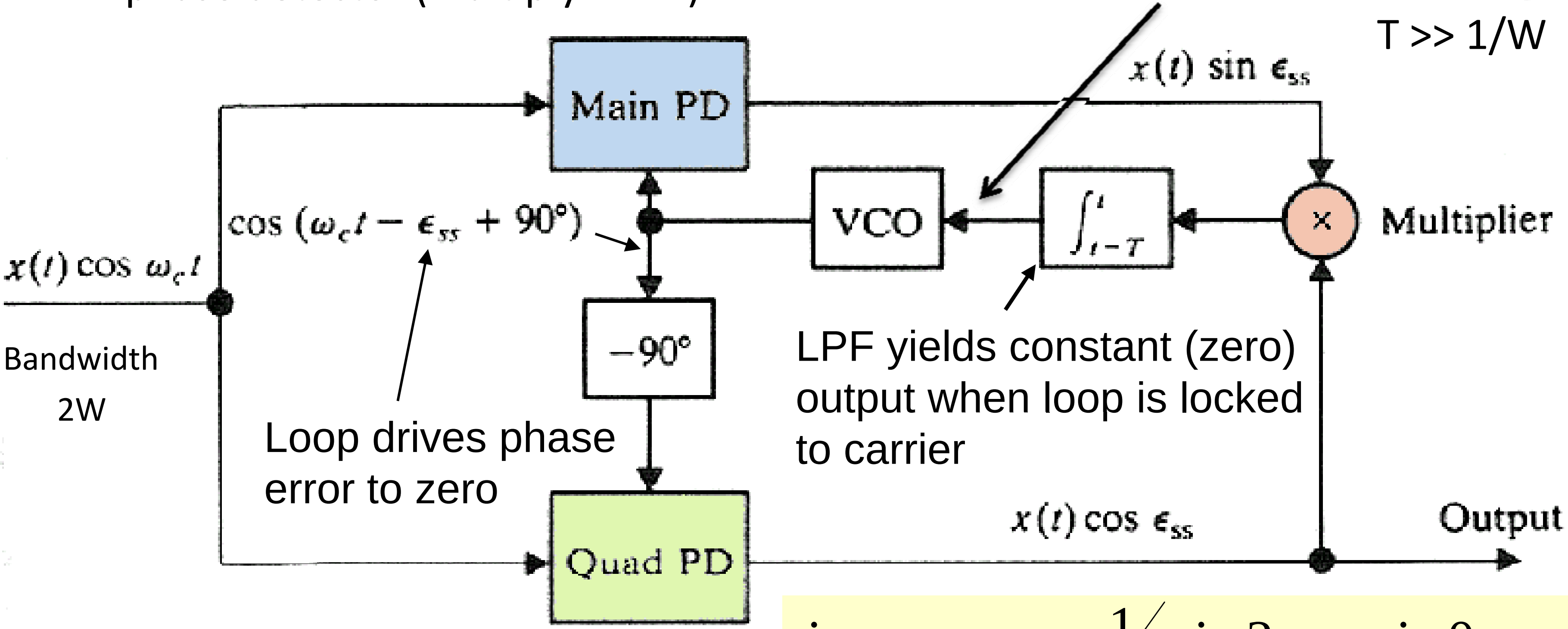
(Assumes unity sinusoids throughout)

Detecting DSB using PLL without pilot

- In ***Costas PLL*** two phase discriminators are used to:
  - Cancel out DSB modulation $x(t)$ in the driving signal
  - Synchronize the output frequency to the center frequency of the DSB spectra (the suppressed carrier), and
  - Detect the DSB signal
    - As when PLL locks ($\varepsilon_{ss} \approx 0$) output → x(t) as cos ε_{ss} → 1

$$y_{ss} \approx T\langle x^2(t)\rangle \sin\epsilon_{ss}\cos\epsilon_{ss} = \frac{T}{2} S_x \sin 2\epsilon_{ss}$$

PD: phase detector (multiply + LPF)



T >> 1/W

Bandwidth
2W

Loop drives phase error to zero

LPF yields constant (zero) output when loop is locked to carrier

$$\sin\varepsilon_{ss}\cos\varepsilon_{ss} = \tfrac{1}{2}\sin 2\varepsilon_{ss} + \sin 0 \approx \varepsilon_{ss}$$

Frequency-offset loop

- Auxiliary oscillator translates frequency (and phase)
  - Of output frequency to $f_c + f_1$
- So free running VCO frequency
  - $f_v = (f_c + f_1) - \Delta f \approx (f_c + f_1)$
- At PLL lock ($\varepsilon_{ss} \approx 0$) input and output of LPF 90^0 out of phase

$$\theta_v(t) - (\omega_1 t + \phi_1) = \omega_c t + \phi_0 + 90^0$$

- VCO produces frequency shifted output