The University of Queensland
School of Information Technology & Electrical Engineering

COMS3100/7100 Introduction to Communications
Semester 1, 2011

Tutorial 8 Solutions

Problem 1

Consider a PLL in steady state with $\varepsilon_{ss} << 1$ for t < 0. The input frequency has a step change at t = 0, so $\phi(t) = 2\pi f_1 t$ for t > 0. Solve eq [5] to find and sketch ε(t), assuming that K >> $|\Delta f + f_1|$.

$\dot{\varepsilon}(t) + 2\pi K \sin \varepsilon(t) = 2\pi\Delta f + \dot{\phi}(t)$	[5]
$K \triangleq K_v K_a$	

Solution:

$t < 0, \quad \varepsilon_{ss} = \Delta f / K$

$t > 0, \quad \phi' = 2\pi f_1$ and $\dfrac{\Delta f + f_1}{K} \ll 1$ so assume $|\varepsilon| \ll 1$ and $\sin\varepsilon \approx \varepsilon$

Thus, $\dot{\varepsilon} + 2\pi K\varepsilon = 2\pi\left(\Delta f + f_1\right) \Rightarrow$ trial solution $\varepsilon = A + Be^{st}$

Then $Bse^{st} + 2\pi KA + 2\pi KBe^{st} = 2\pi\left(\Delta f + f_1\right)$

$$\text{so} \quad \left.\begin{aligned} 2\pi KA &= 2\pi\left(\Delta f + f_1\right) \\ (s + 2\pi K)Be^{st} &= 0 \end{aligned}\right\} \Rightarrow \begin{cases} A = \dfrac{\Delta f + f_1}{K} \\ s = -2\pi K \end{cases}$$

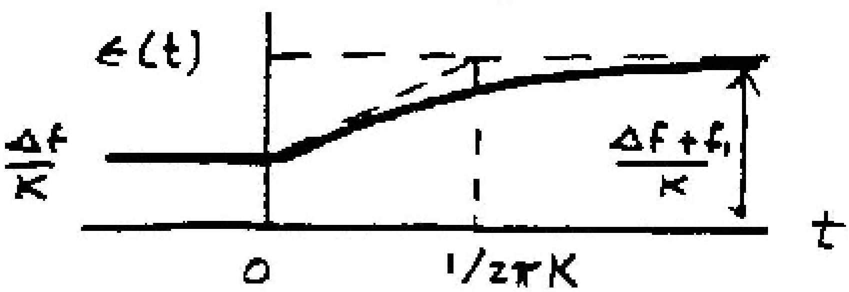
and $\varepsilon(t) = \dfrac{\Delta f + f_1}{K} + Be^{-2\pi Kt}, \quad t > 0,$

Since $\varepsilon(t)$ can make a step change at $t = 0$,

$$\varepsilon(0^+) = \frac{\Delta f + f_1}{K} + B = \varepsilon(0^-) = \frac{\Delta f}{K} \Rightarrow B = -\frac{f_1}{K}$$

Hence,

$$\varepsilon(t) = \begin{cases} \dfrac{\Delta f}{K} & t < 0 \\ \dfrac{\Delta f}{K} + \dfrac{f_1}{K}(1 - e^{-2\pi Kt}) & t > 0 \end{cases}$$



Problem 2:

Modify the FM stereo receiver in Fig. 7.2-5 to incorporate a PLL with $f_v \approx 38$kHz for the subcarrier. Also include a dc stereo indicator.

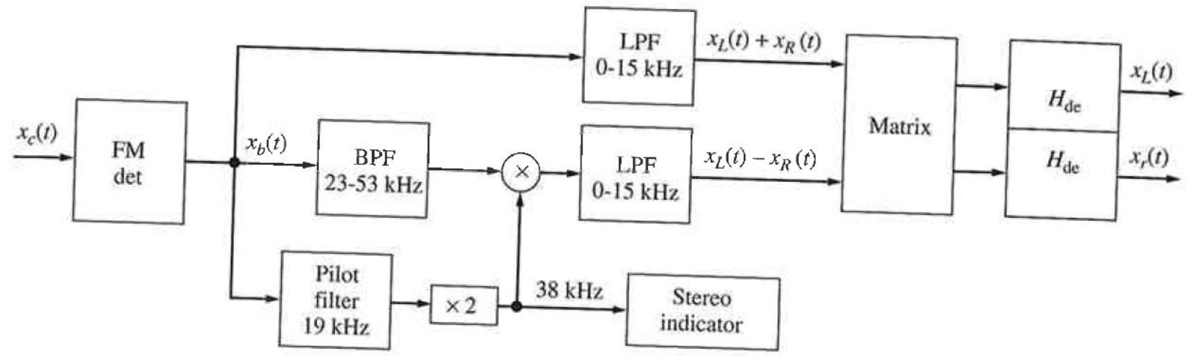
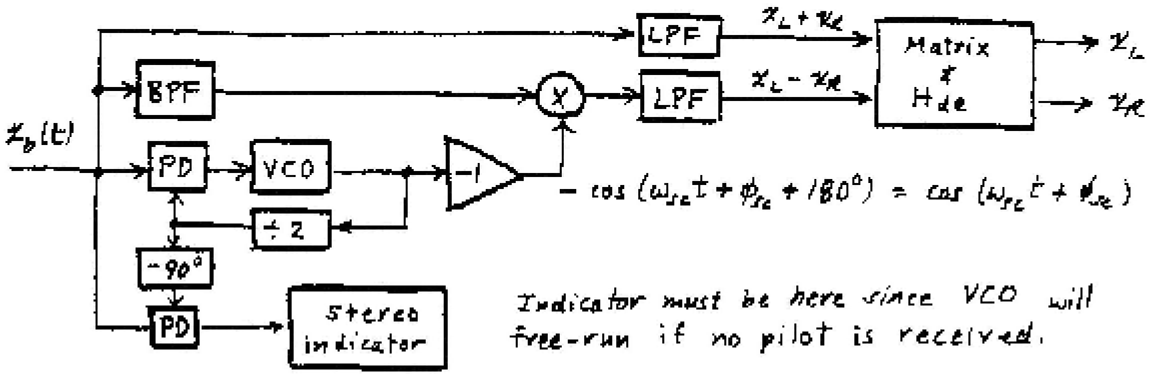


Figure 7.2-5 FM stereo multiplex receiver.

Solution:

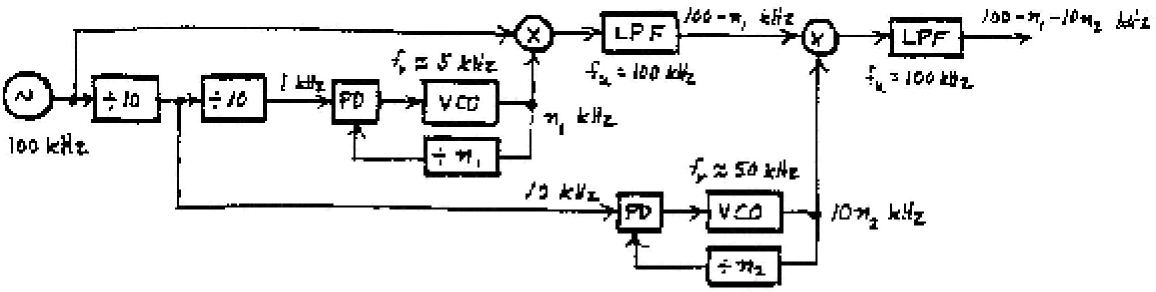
Let subcarrier be $\cos(\omega_{sc}t + \phi_{sc})$ so pilot signal is $\cos\left[(\omega_{sc}t + \phi_{sc})/2\right]$
and output of PLL doubler will be $\cos\phi_v(t) = \cos\left[2(\omega_{sc}t + \phi_{sc})/2 + 2 \text{ x } 90^0\right]$



Problem 3:

Given a 100 kHz master oscillator and two adjustable divide-by-n counters with n = 1 to 10, devise a system that synthesizes any frequency from 1kHz to 99kHz in steps of 1 kHz. Specify the nominal free-running frequency of each VCO.

Solution:



f_v = 5kHz, 50kHz

Problem 4:

Referring to Table 7.1-1, devise a frequency synthesizer to generate $f_{LO} = f_c + f_{IF}$ for an FM radio. Assume you have available a master oscillator at 120.0 MHz and adjustable divide-by-n counters with n = 1 to 1000.

Parameter	FM
Carrier frequency	88.1-107.9 MHz
Carrier spacing	200 kHz
Intermediate frequency	10.7 MHz
IF bandwidth	200-250 kHz
Audio bandwidth	15 kHz

Table 7.1-1

Solution:

$f_{LO} = f_c + f_{IF}$ = 98.8 to 118.6 MHz in steps of 0.2 MHz = 120.0 MHz ÷ 600

120.0 - 98.8 = 106 x 0.2 MHz, 120.0 - 118.6 = 7 x 0.2 MHz