

CSSE4000/7002 Digital System Design II

Introduction to System-on-Chip

Motivation

- Technological Advances
 - today's chips can contain >150M transistors
 - transistor gate lengths measured in nanometers
 - approximately every 18 months the number of transistors on a chip doubles – Moore's law

[Shini]

[Lockwood]

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Motivation

- The Consequences
 - components connected on a Printed Circuit Board can now be integrated onto single chip.
 - hence the development of System-On-Chip design.

From PCB to SoC

[Shini]

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Motivation

- The productivity gap
 - Semiconductor *technical capabilities* outpace industry *design capabilities*

How to design a system with 200M transistors?

Year	Technology	Chip Complexity	Transistors	1 Yr. Design Staff	Staff Cost*
1987	250 nm	43 M Tr.	400	250	\$9 M
1988	250 nm	29 M Tr.	500	270	\$120 M
1999	180 nm	32 M Tr.	600	360	\$160 M
2002	130 nm	130 M Tr.	800	800	\$360 M

* @ \$150K / Staff Yr. (in 1997 Dollars)

[Sander]

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To market, to market

Time-to-market directly influences time-in-market, which impacts revenue

[Sander]

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Design Re-Use

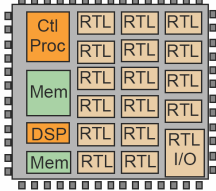
One chip → Many system designs

[Sander]

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What is SoC?

- Not only the silicon
 - Emphasis on "system".
 - SoC = Chip + Software + Integration
- The SoC chip includes:
 - Embedded processor(s)
 - Interconnect
 - ASIC Logic and analog circuitry
 - Embedded memory



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What is SoC?

- SoC software includes:
 - Operating system
 - Compilers, linker, debugger, IDE
 - Simulators
 - Firmware, bootloaders
 - Drivers
 - Protocol stack
 - Application interface (C/C++, assembly)
- Don't forget application code!

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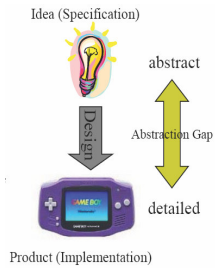
What is SoC?

- SoC integration includes
 - The whole system solution
 - Manufacturing consultant
 - Technical support
 - Test and verification

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How to design an SoC?

- Specification
 - Design productivity increases with level of abstraction
 - Functional verification is very difficult at low abstraction levels
- Implementation
 - Efficient implementations mean exploiting low-level features of the target architecture



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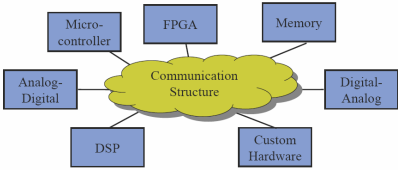
Efficient System Design

- Design time shortened by
 - Increased level of *abstraction*
 - Tool support* to automate transformation from high-level specification to low-level implementation
 - Platform architectures* with optimized components and communication structures

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SoC Architectures

- Integrates several *heterogeneous components* on a single chip



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Bus-based architectures

The diagram illustrates a bus-based architecture. A central horizontal line represents the 'System Bus'. Above this bus, three components are connected: a Microprocessor (light blue), a DSP (purple), and Custom / programmable logic (orange). Below the bus, two more components are connected: Memory (light blue) and IO (grey). All components are connected to the bus via vertical lines.

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Network-on-Chip Architectures

The diagram illustrates a Network-on-Chip (NoC) architecture. It features a central network of yellow 'Switch/routers' connected by blue lines. Three components are connected to the network via grey 'NIC' (Network Interface Card) blocks: a Microprocessor (light blue), a DSP (purple), and Custom / programmable logic (orange). Memory (light blue) and IO (grey) are also connected to the network via their own NIC blocks.

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SoC Components

- o IP (intellectual property) cores
 - Drop-in modules offering specific, verified functionality
 - Test benches
 - Device drivers
- o Deliverable formats
 - VHDL / Verilog
 - Pre-synthesised netlists
 - Pre-mapped cells/macros
- o Integration still a major engineering task

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SoC Components

- o Component architecture
 - Processors
 - Buses
 - Memory and interfaces
 - On-chip and off-chip
 - IO devices

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Processors

- o Dominant SoC CPU architectures
 - ARM
 - MIPS
 - PowerPC
 - Cell / PS3
 - x86
- o Others
 - Motorola Coldfire
 - Various FPGA-based CPU architectures
 - Xilinx MicroBlaze, Altera NIOS / NIOS II

<http://linuxdevices.com/articles/AT4313418436.html>

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Buses and interconnect

- o Many standards
 - AMBA (ARM)
 - Wishbone
 - CoreConnect (IBM / PowerPC)
 - Xilinx FPGA-based SoC platforms
- o Design choices
 - Structure (flat vs heirarchical)
 - Clocking (synchronous vs asynchronous)
 - Arbitration (centralised vs distributed)

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Memory and Interfaces

- Digital logic and large or nonvolatile memories don't mix nicely
 - SoC architectures tend to provide limited on-chip memory and common off-chip interface cores
- On-chip memory
 - Fast access (1 or 2 cycles)
 - Limited capacity
 - 100's of kbit / a few Mbit
- Off-chip memory
 - SRAM, DRAM, Flash
 - Slower access (5-15 cycles)
 - Much greater capacity
 - Megabytes -> Gigabytes

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I/O Interfaces

- Enormous variety
 - Application domain dependent
- Common features
 - GPIOs
 - Serial, ethernet, wireless
 - Audio/display drivers
 - Consumer interfaces
 - USB, SDIO, ...
 - Imaging sensors
 - Mass storage (CF, MMC)
 - Inter-chip interfaces (SPI, I²C)

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Other Components

- Clock and time management
 - Clock multipliers, dividers
 - Timers, counters
 - Watchdog timers
 - Real time clocks (RTC)
- Application accelerators
 - Multimedia encode/decode
 - Graphics engines
 - Ethernet/IP switches
- Power management

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Implementation Technologies

	Initial cost	Cost per part	Performance	Fabrication time
FPGA	Low	High	Low	Low
Standard cell				
Full custom	High	Low	High	High

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Design Process

- Mapping a design specification to an architecture

```

graph TD
    DS[Design specification] --> DP[Design process]
    AS[Architecture specification] --> DP
    DP --> DI[Design implementation]
  
```

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Design process (uniprocessor example)

- Source code compiled and linked to run on a CPU + operating system

```

graph TD
    PCT[Program code (parallel tasks)] --> CL[Compile + Link]
    UOS[Uniprocessor + operating system] --> CL
    CL --> EC[Executable code]
  
```

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Design Process

- Typical SoC design process is much more complicated
 - Many parallel tasks
 - Multiple processing elements
 - Many possible mappings – which to choose?
 - Communication overheads
 - Realtime deadlines
- Design must choose appropriate architecture and appropriate mapping
 - How to manage the complexity?

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Design Process

- Several approaches
 - Platform-based design
 - SoC vendors provides a common platform
 - Programmer's model
 - Software libraries
 - Tools
 - Design examples
 - Hardware / Software Co-design
 - See this week's reading

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Summary

- SoC is
 - A necessity
 - A technology
 - A design approach
 - An evolving field

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For next week

- Read the reading – “Hardware Software Co-Design”
 - Discussion questions will be published tomorrow
 - Talk about it in next week's tut
- Lab sessions start next week

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