

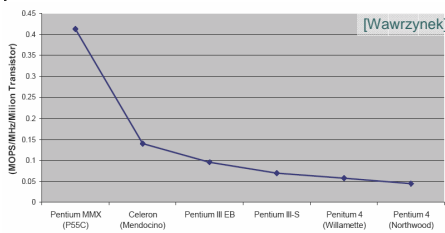
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Introduction to Reconfigurable Computing

Computational density

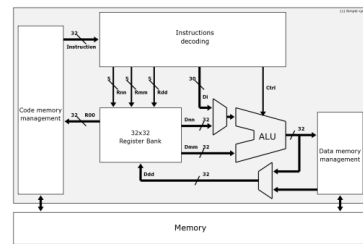
- Moore's law
 - more transistors per die
 - higher clock speeds
 - higher power!
- What about efficiency?
- How much computational "work" do we get out of each transistor?
- Computational density
 - Computation per transistor per Mhz

Computational density



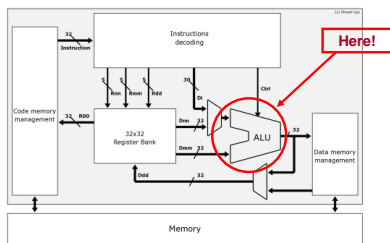
Is this a good trend?

Thinking about CPUs



Q: Where does the computational work occur?

Thinking about CPUs



A: The ALU

Thinking about CPUs

- The example is a **really** simple CPU architecture
- What about a modern CISC CPU like a Pentium?
 - branch prediction, instruction reordering
 - Intel "Prescott" has 31 pipeline stages!
 - Caches, MMU
- Literally millions of transistors who's job is to get data to the ALU / FPU
 - Time multiplexing the ALU resource

Thinking about CPUs

“Are we making copies in sub-micron CMOS VLSI of copies in NMOS of copies in TTL of early vacuum tube computer designs?”

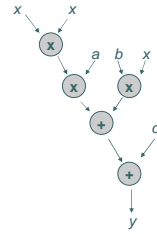
Andre DeHon

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Spatial Computing



- Consider the function
 - $y = ax^2 + bx + c$
- A hardware resource is allocated for each operator
- The computation graph can be implemented directly

[after Wawrzynek]

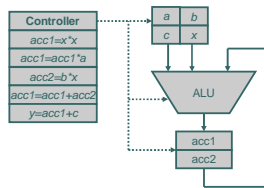
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Temporal Computing

- A hardware resource (ALU) is time-multiplexed by a controller
- Similar to a software / CPU solution
- There is a spectrum between pure sequential and pure temporal computing



[after Wawrzynek]

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Spatial vs temporal

- Create both spatial and temporal computing designs for compute a 3-tap FIR filter:

$$y[i] = ax[i] + bx[i-1] + cx[i-2];$$

$$x[i] = x[i-1]$$

- Notes

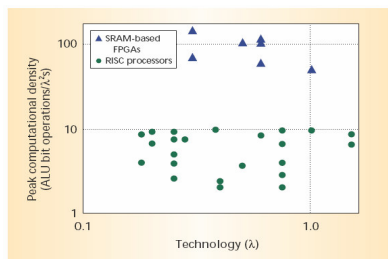
- Use a register pipeline to hold the “history” of $x[i..i-2]$ in the spatial version
- Use 2-input multipliers/adders only

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Computational Density



[DeHon]

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Instruction binding time

- When is the decision made of which operation to perform?

[Wawrzynek]

	“hardware”			“software”	
Media:	Custom VLSI	Gate Array	One-time prog.	FPGA	CPU
Binding Time:	First mask	Metal mask layers	Fuse program	Config. time	Every cycle

Later binding time →

In general – the earlier the decision is bound, the less area and delay required for the computation

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Reconfigurable Computing

- One possible definition
 - “Computing via a post-fabrication and spatially programmed connection of processing elements” (Wawrzynek)
 - FPGA implementation of CPU excluded – not a spatial mapping
 - ASIC implementations excluded – not post-fab programmable
 - What about arrays of processors?

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Economics (again)

- Costs:
 - Unit cost – cost of manufacturing each item, excluding NRE
 - NRE (non-recurring engineering) cost: One time monetary cost of designing the system
 - $total_cost = NRE + unit_cost * num_units$
 - $per_product\ cost = \frac{Total_cost}{num_units} = (\frac{NRE}{num_units}) + unit_cost$
- Example
 - $NRE = \$2000, unit_cost = \100
 - For 10 units
 - $Total_cost = 2000 + 10 * 100 = \3000
 - $Per_product = 2000/10 + 100 = \300

[Vahid]

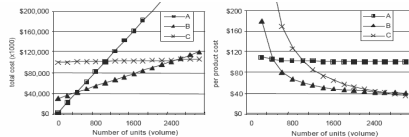
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Economics

- This analysis allows comparison of technologies, e.g.
 - Tech A: $NRE = \$2,000, unit_cost = \100
 - Tech B: $NRE = \$30,000, unit_cost = \30
 - Tech C: $NRE = \$100,000, unit_cost = \2



Per-product cost depends on number of units sold [Vahid]

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Economics of RC

- ASIC: High NRE costs, low cost per die
- FPGA: Low NRE, high cost per device
 - Design-effort NRE still must be considered
- Trends
 - ASIC NRE growing dramatically
 - FPGA cost per device decreasing
 - The crossover point is moving steadily to the right (increasing volume)

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An example

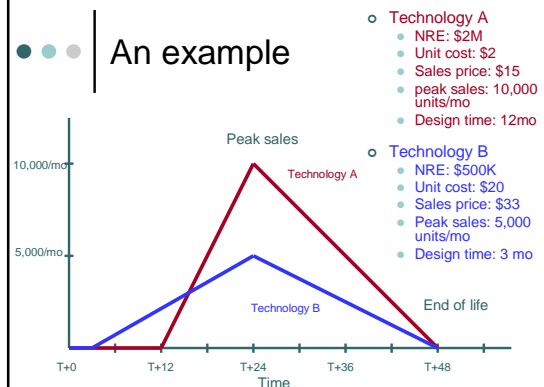
- Designing and selling a widget
 - Start now (T+0)
 - Peak sales at T+24mo (market saturation and competition)
 - End of life T+48mo (obsolete)
 - Which technology to use?
- Technology A
 - NRE: \$2M
 - Unit cost: \$2
 - Sales price: \$15
 - peak sales: 10,000 units/mo
 - Design time: 12mo
- Technology B
 - NRE: \$500K
 - Unit cost: \$20
 - Sales price: \$33
 - Peak sales: 5,000 units/mo
 - Design time: 3 mo

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An example



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Other drivers for RC

- Risk management
 - Resilience against late design changes
 - Tolerance to design and manufacturing faults
- Flexibility
 - Generic platform with multiple “personalities”
 - In-the-field upgrades of hardware, not just software (patching the hardware)
 - Product life extension

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Dynamic Reconfiguration

- FPGAs are **re**-configurable
 - Time-multiplexing the hardware
 - Run-time circuit specialisation
- Partial reconfiguration
 - Reconfigure only part of the logic fabric, while the rest continues to operate
- Largely research/experimental stages
 - Software-Defined Radio (SDR) is a new industry driver

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Dynamic Reconfiguration

- Challenges
 - (Re-)configuration time
 - Tools
- Opportunities
 - constrained size/weight
 - multiple ASICs are too big/expensive, processors too slow
 - Reducing physical inventory

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Advantages of RC

- Computational density
- Allows designers to match architecture to the application
- Encourages fine-grained parallelism
- Dynamic reconfiguration and hardware multiplexing?

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Challenges for RC

- Design effort
 - Tools
 - Early stages for true RC tools
 - Existing tools look like traditional HW design
- Power consumption
- Device and tool support for dynamic reconfiguration

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Reading this week

- DeHon – “The Density Advantage of Configurable Computing” IEEE Computer, April 2000

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Reconfigurable Scalable Computing (RSC)

- Modular, FPGA-based space computing platform
- Motivated by the push towards on-board computing
- Generic hardware modules
 - Reduce inventory
 - Thermal/mechanical testing



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References

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 - CSE 566 Lecture notes
 - <http://www.arl.wustl.edu/~lockwood/class/cse566-f04/>
- John Wawrzynek – Berkeley
 - CS294-3 Reconfigurable Computing Lecture Notes
 - <http://www-inst.eecs.berkeley.edu/~cs294-3/sp04/>
- Frank Vahid
 - Embedded Systems Design: A Unified Hardware/Software Introduction

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