
CSSE4000/7002

Digital Design II

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Course website:

<http://www.itee.uq.edu.au/~csse4000>

<http://www.itee.uq.edu.au/~csse7002>

Objective of this Subject

- ◆ To gain an understanding of VLSI circuits:
 - Design
 - Analysis
 - Problem/Issues
- ◆ To gain the ability to design small digital systems in VLSI technology using commercial CAD tools.
- ◆ To gain experience with system design on FPGA.

Requirements

BACKGROUND:

- ◆ CSSE2000:
 - Basics of electronic devices
- ◆ CSSE3000:
 - Basics of digital system design and theory
 - Basics of FSM based controller design

VLSI Project

- ◆ Objective: learn the process of VLSI design
- ◆ Design a CMOS combinational logic circuit as a complex CMOS gate
- ◆ Layout, route, calculate parameters and parasitics, estimated performance, report
- ◆ Done via Mentor Graphics IC-Station tools

2nd Project

- ◆ A number of choices
- ◆ More information will be made available in coming weeks

Assessment

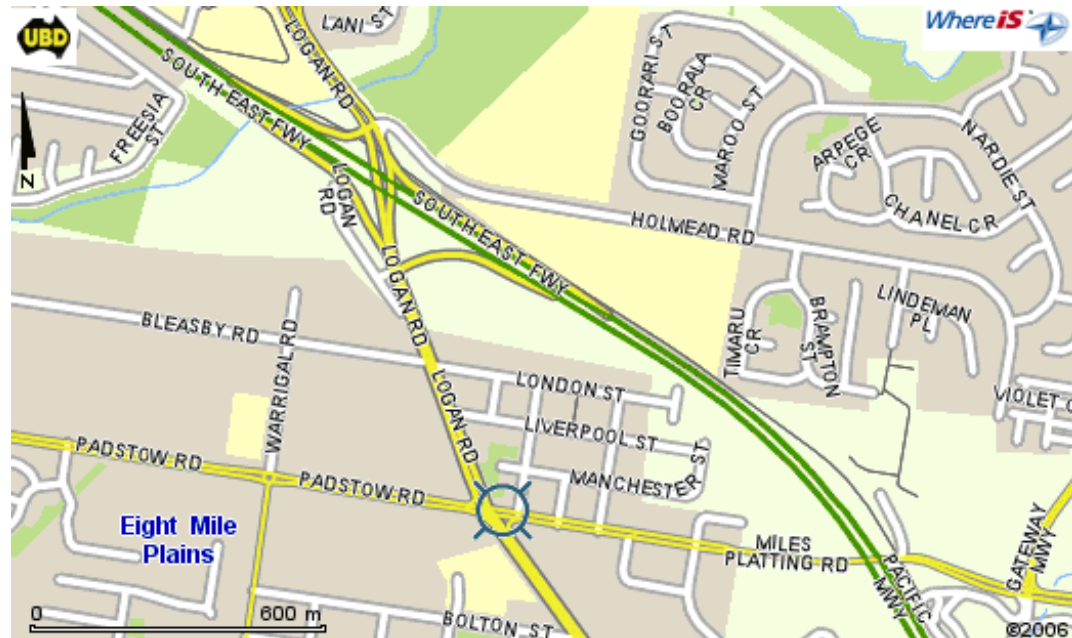
◆ Design project I - VLSI	30%
◆ Design project II - HDL/FPGA	30%
◆ Final examination (2 hours)	40%
– Questions from the whole course	
– Tutorials questions will aid final exam	
TOTAL	100%

Textbook(s)

- ◆ Textbook: Jan Rabaey, “Digital Integrated Circuits – A design perspective”, Prentice Hall, ISBN 0-13-394271-6
- ◆ Reference : Any other book on VLSI design
(but READ it!)
- ◆ Later: any HDL books, XILINX WEB pack if your 2nd project relates to HDL

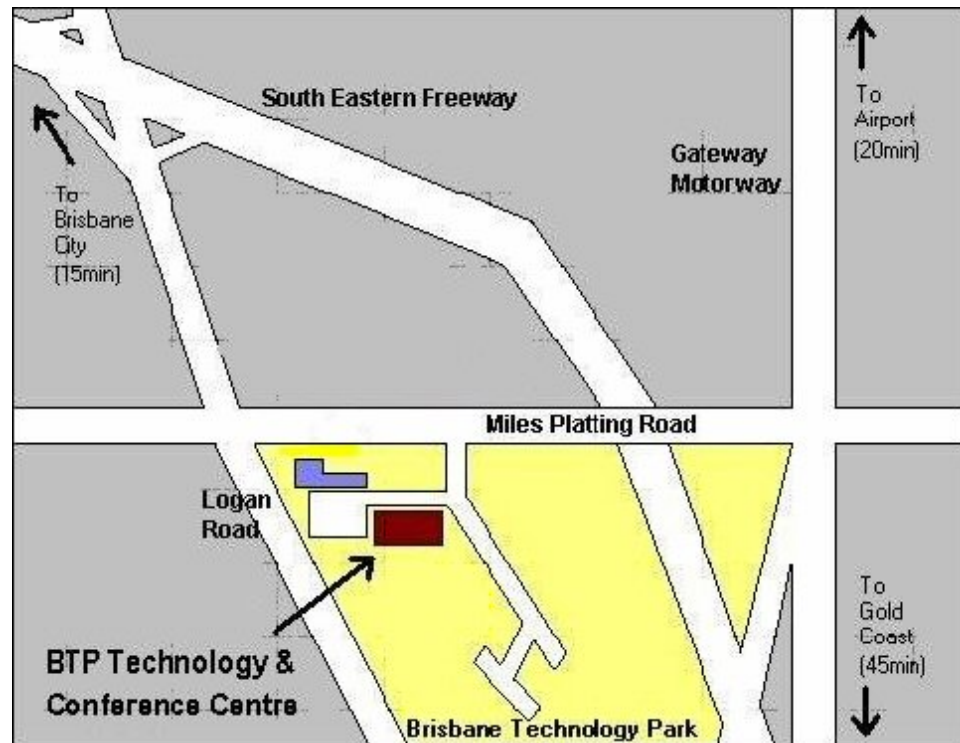
Venue

- ◆ All Contact Sessions to be moved to:
- ◆ Australian Microelectronic Centre
 - CAD Tools + Companies



More about the Venue

- ◆ Plenty of Car Parks & Busway near by.



Timetable Suggestion

- ◆ Originally:
 - Lecture (Fri) 12 to 2pm
 - Prac (Mon) 2 to 4pm
 - Tut (Mon) 4 to 6pm
- ◆ Suggested New Times:
 - Lecture (Mon) 1 to 3pm
 - » starting week 2, ie. 31 July
 - Prac + Tut (Mon) 3 to 6pm
 - All contact sessions are at AMC!

Questions?

- ◆ Any questions?
- ◆ Short break
 - 5 min
 - Organise transport with your peers