


CSSE4000 / CSSE7002 Digital System Design II


Reconfigurable System-on-Chip Component
John Williams
jwilliams@itee.uq.edu.au



Course delivery

- Lecturer
 - Dr John Williams
(jwilliams@itee.uq.edu.au)
- Contact hours
 - Mondays 1-6pm at AMC Facility
 - Weeks 7-13
 - Other times by appointment only


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Objectives

- Demonstrate understanding of
 - concepts of system on chip, reconfigurable computing and reconfigurable system on chip
 - economic factors in rSoC design
 - phases of the design process
 - tradeoffs vs ASIC / standard cell / full custom
 - building blocks of rSoC architecture
 - architectural issues in rSoC architecture


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Practical outcomes

- Develop simple systems using the Xilinx Embedded Development Kit (EDK)
- Develop simple custom system components (IP core) and integrate with rSoC
- Simulate rSoC systems at different levels of simulation granularity


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Course delivery

- Lectures
 - Three weeks of lectures
- Readings
 - One or two readings set for each lecture
 - You are expected to read these!
 - Class discussions each week
- Tutorials/pracs
 - Self-paced – learning the Xilinx System-on-Chip design tools
 - JW and tutor available for assistance
- Course material
 - Lecture slides will be available on the web
 - Tutorial/prac material will be provided as required

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Assessment

- Assignment (30%)
 - Investigate tradeoffs in HW vs SW design for implementing custom SoC functionality
 - Handed out next week (week 8)
 - Due week 13
- Questions on final exam

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Course overview

- Week 7 - Introduction to System-on-Chip Design
 - Motivation
 - Component architectures
 - Design approaches
- Week 8 - Introduction to Reconfigurable Computing
 - What is it?
 - Spatial vs temporal computing
 - Technical and economic motivators
- Week 9 - Reconfigurable System-on-Chip
 - Best of both worlds / worst of both worlds?
 - Architectural considerations