

## CSSE4000/7002

### Revision questions covering the material to be examined in the final examination

1. Design a multistage CMOS buffer
  - a. Given input capacitance and the load capacitance calculate the number of stages. Use either the theoretically optimal buffer stage scaling or practical value. Comment on why the practical value differs from the theoretical.
  - b. Given equivalent resistances of minimum size PMOS and NMOS transistors, their gate capacitance and drain bulk capacitance calculate sizes of transistors in the stages, and stage capacitances.
  - c. Calculate the total delay through the buffer for falling and rising signals
  - d. Estimate the area of the last stage of the buffer given the technology rules in lambda units. (fold the transistors)
  - e. Explain the importance of multiple via connecting the transistors
  - f. Optimise the delay of a chain or network of inverters - See example problem 5.5 P.210 on Rabaey.
  
2. Given the technology parameters and MOS transistors equations:
  - a. calculate gate source capacitance of the transistor
  - b. calculate drain bulk capacitance of the transistor
  - c. calculate capacitance and resistance of given polygon of poly or metal
  - d. explain why MOS transistor in saturation is treated as current source
  - e. explain the relation between the width of the transistor and its resistance
  - f. explain the ways the power is consumed in CMOS
  
3. Design a CMOS circuit (complex gate), either static or dynamic, implementing a given Boolean expression
  - a. Produce the transistor schematic, minimize the number of transistors
  - b. Draw the stick diagram
  - c. Define the rising and falling delays for the circuit
  - d. Calculate those delays, given minimum size transistor parameters
  - e. Scale the transistors for symmetrical output
  - f. Scale the transistors for speed
  - g. Optimize position of the transistor carrying given critical path signal
  
4. Design styles
  - a. What are the differences between static CMOS, dynamic CMOS & transmission gate design
  - b. What are the advantages and disadvantages of those designs?
  - c. What are the advantages and disadvantages of pass transistor style, why transmission gate is better, when are voltage level restoring circuits needed?
  - d. Why pull down is always made of NMOS transistors and pull up of PMOS in CMOS technology
  - e. What is the essential difference between dynamic CMOS and static in terms of power consumption?
  - f. Is dynamic CMOS quicker? Why or why not?
  
5. Dealing with interconnect :
  - a. explain the effects of capacitance and resistance of interconnect on the performance of circuits
  - b. explain why higher level metal layers are better for global signals such as clock and power network
  - c. how to decrease interconnect delay through technology

- d. What is the Elmore Delay of an interconnect?
  - e. how to decrease delay of long wires
  - f. show a layout of good power distribution network
6. Sequential logic
- a. Show how to calculate the maximum clock frequency in the sequential system (such as FSM)
  - b. Define the clock skew; explain the potential problems created by excessive clock skew.
  - c. Produce circuit diagrams of a static CMOS latch and a dynamic CMOS latch. Compare the storage mechanism, the advantages and disadvantages of both.
7. SOC Designs
- a. See lectures regarding SOC
8. Building Blocks - adders
- a. What are the circuits used for making adders?
  - b. Draw block diagrams of these adders and explain their operations.
  - c. List their advantages and disadvantages.
9. Building Blocks - memories
- a. Identify the differences (structural & operational) of SRAM and DRAM.
  - b. What are the building blocks of SRAM & DRAM?
  - c. What are the circuits used to store binary values in SRAM & DRAM?
  - d. What supporting circuitries are also found in SRAM & DRAM structures?
  - e. Why do we need sense amplifiers in the memory structure?
  - f. Why is DRAM preferred over SRAM for the use of main memory in personal computers?
  - g. Why is SRAM used as cache in the recent microprocessors?
10. Other Building Blocks
- a. What is a phase-lock loop?
  - b. What is a delay-lock loop?
  - c. Draw block diagrams for each and explain their operations.