CSSE4000/7002 Tutorial 1

Problem Set for Lecture 1 and 2

1. Visit the Intel online microprocessor museum (http://www.intel.com/museum). Find the "microprocessor hall-of-fame", and use the information there, as well as the quick reference guides and/or other links, to determine the rate of increase in transistor counts every 5 years since 1970 for Intel processors.

2. If you are asked to design ICs for an application targeted at consumers, what are the engineering issues that governs the success or the failure of your design? What other issues must you consider as well?

3. What does the term NRE cost of an IC mean? Recurrent costs of an IC?

4. Describe the photo-lithographic process used to manufacture CMOS IC.

5. Identify the steps/setup/work cost in the lithographic process which contributes to the NRE cost of making an IC. Also identify those which contribute to the recurrent cost.

6. If a mistake is made on the design stage, the mask layout, how is the NRE and recurrent cost affected?

7. Name the bonding techniques used in IC packaging.

8. Draw a 3 input CMOS OR gate schematic. Draw a stick diagram for this gate. Create a layout of this gate using graph paper (or similar) with the colour conventions shown in lectures.

9. Draw a 2-input AND gate timing diagram with all possible input combinations and outputs waveform. Use this diagram to define the rise time, fall time, low-to-high delay and high-to-low delay of this gate.