

**FINAL PROGRAMME**

	September 4, Tuesday	September 5, Wednesday	September 6, Thursday	
9.00	<p><b>Opening Session</b> (common with Euromicro) Chair: <i>Lech Józwiak</i> <b>Addresses:</b></p> <p>Representative of Polish Government,  <i>Prof. dr. hab. Roman Morawski,</i> Dean of the Faculty of Electronics and Information Technology, Warsaw University of Technology</p> <p><i>John Moelgaard,</i> President of Euromicro</p> <p><b>Keynote:</b> Power - The Next Frontier, <i>Ronny Ronen, Intel</i></p> <p><i>Janusz Sosnowski -</i> <b>Organizational Issues</b></p>	<p><b>Reconfigurable Computing</b> Chair: <i>Adam Postula</i></p> <p><b>Keynote:</b> Reconfigurable Computing at Xilinx, <i>Steve Guccione, XILINX.</i></p> <p><b>Keynote:</b> Reconfigurable Computing: a New Business Model and its Impact on SoC Design, <i>Reiner W. Hartenstein, Uni of Kaiserslautern.</i></p>	<p><b>Reversible Logic</b> Chair: <i>Lech Józwiak</i> <b>Tutorial:</b> Fundamentals Of Reversible Logic And Computing, <i>M.Perkowski, P.Kerntopf</i></p> <p>Regular Realization of Symmetric Function using Reversible Logic, <i>M.Perkowski et al.</i></p>	<p><b>Specialised Architectures</b> Chair: <i>Steve Guccione</i></p> <p>Rotating Ultrasonic Signal Vectors with a Word-Parallel CORDIC Processor, <i>A.Papliński, N.Bhattacharjee</i></p> <p>FPGA implementation of a faithful polynomial approximation for powering function computation, <i>J.Piñero et al.</i></p> <p>Cork Stopper Classification Using FPGAs and Digital Image Processing techniques, <i>M. A.V. Rodriguez et al.</i></p> <p>Pipelining considerations for an FPGA case, <i>O.Cadenas, G.Megson</i></p>
10:30	Coffee break	Coffee break	Coffee break	

11.00	<p><b>Keynote session</b> Chair: <i>Antonio Nunez</i></p> <p>Design-for-Test Challenges of Complex SoC Designs, <i>Janusz Rajski, Mentor Graphics</i></p> <p>Keynote Speech from <i>Nokia</i></p>	<p><b>Reconfigurable Computing</b> Chair: <i>Rolf Ernst</i></p> <p>Design And Implementation Of Reconfigurable Processor For Problems Of Combinatorial Computations, <i>I.Skliarova, A.B.Ferrari</i></p> <p>Optimisation of PPMC Model for h / w Implementation, <i>C. Feregrino</i></p> <p>Traffic Scheduling Coprocessor with Schedulability Analysis Capability, <i>E. Martins, J.A.Fonseca</i></p> <p>A Run-Time Support Environment for Reconfigurable Systems, <i>L.Bubb, M.Edwards et al.</i></p>	<p><b>Synthesis and verification Posters</b> Chair: <i>Rolf Drechsler</i></p> <p>An improved input-output encoding approach for functional decomposition, <i>M. Venkatesan</i></p> <p>Level assignment for displaying combinational logic, <i>R. Drechsler et al.</i></p> <p>Decomposition of Boolean Functions Targeted to Multiplexing, <i>V.Tomaszew</i></p> <p>System Modeling in the COSMA Environment, <i>W.Daszczuk et al.</i></p> <p>Evaluation of Temporal Formulas Based on "Checking by Spheres" <i>W.Daszczuk</i></p> <p>Applying Formal Verification with Protocol Compiler, <i>C. Stangier</i></p> <p>Synthesis of sequential circuits on Programmable Logic Devices based on models of finite state machines, <i>V.Solovjev</i></p>	<p><b>Synthesis</b> Chair: <i>Adam Pawlak</i></p> <p><b>Invited paper:</b> Very High (Over 40 Gb/S) Speed Circuits For Optical Communication, <i>A. Kończykowska French Telecom R&amp;D)</i></p> <p>On the Capabilities of Redundancy Addition and Removal for Sequential Logic Optimization <i>E.San Millan, L.Entrena, J.A.Espejo</i></p> <p>On the Use of Mutations in Boolean Minimization, <i>P.Fišer, J.Hlavička</i></p>	<p><b>Test and design for testability</b> Chair: <i>Raimond Ubar</i></p> <p>Evaluation of Delay Fault Testability of LUT Functions for Improved Efficiency of FPGA Testing, <i>A.Krasniewski,</i></p> <p>Fast Test Cost Calculation for Hybrid BIST in Digital Systems, <i>R.Ubar et al.,</i></p> <p>Test Strategies On Functionally Partitioned Module-Based Programmable Architecture For Base-Band Processing, <i>S.Leung, A.Postula</i></p>
12.30	LUNCH	LUNCH	LUNCH	LUNCH	LUNCH

14.00	<p><b>System Design</b> Chair: <i>Martyn Edwards</i></p> <p><b>Invited paper:</b> Header Compression in Handel-C - An internet HW application and a new design language", <i>Kjell Torkelsson, Ericsson</i></p> <p>A Multi-lingual Synthesis and Verification Environment, <i>G. Economacos</i></p> <p>A design methodology for high performance IC's: wireless broadband radio baseband case study, <i>V. Aue et al.</i></p> <p>Application of Decision Making Method for Architecture Selection of ADSL Modem, <i>J.P Soinien</i></p>	<p><b>Logic Synthesis</b> Chair: <i>Tadeusz Luba</i></p> <p>Effective and Efficient FPGA Synthesis through Functional Decomposition Based on Information Relationship Measures, <i>L.Józwiak, A. Chojnacki,</i></p> <p>Practical Aspects of Logic Synthesis Based on Functional Decomposition, <i>M.Rawski et al.</i></p> <p>Fast and Compact Sequential Circuits Through The Information-based Circuit Synthesis, <i>L. Józwiak, A.S.Ślusarczyk, A. Chojnacki</i></p> <p>Greedy_IIP: Partitioning large graphs by greedy iterative improvement, <i>B.Becker et al.,</i></p>	<p><b>PANEL: Reconfigurable Computing</b> Chair: <i>Lech Józwiak</i></p> <p>Rainer Hartenstein, Steve Guccione, Rolf Ernst, Kjell Torkelsson, Adam Postula.</p>	<p><b>Processor Design</b> Chair: <i>Janusz Sosnowski</i></p> <p>Design of a Faithful LNS Interpolator, <i>M.Arnold,</i></p> <p>Architectural design of a fast floating-point multiplication-add fused unit using signed-digit addition, <i>C.Chen, C.J.Cheng</i></p> <p>High Performance Floating Point Divide, <i>A.A. Liddicoat, M.J.Flynn</i></p>	<p><b>Specialised architectures Posters</b> Chair: <i>Kjell Torkelsson</i></p> <p>An Assesment of FPGA Suitability for Implementation of Real-Time Motion Estimation, <i>A. Ryszko, K. Wiatr</i></p> <p>Portable Acquisition System for Measurements of Pressures, Temperatures and Humidity in Lower Limb Prosthesis, <i>G. Coldani et al.</i></p> <p>A MIMD based Multi Threaded Real-Time Processor for Pattern Recognition, <i>J. de Cuveland et al.</i></p> <p>Synchronizing a High-Speed SIMD Processor Array, <i>S. Lund, L.Bengtsson</i></p> <p>Pipelined Genetic Architecture with Fitness on the Fly, <i>F.Sáenz et al.</i></p> <p>A wireless interconnection network for parallel processing, <i>J.Marczynski, D.Tabak</i></p>
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15.30	Coffee break		Coffee break		Coffee break	
16.00	<p><b>Embedded systems</b> Chair: <i>Krzysztof Kuchcinski</i></p> <p><b>Tutorial:</b> Combining languages in embedded system design, <i>Rolf Ernst (Uni of Braunschweig)</i></p> <p>Hierarchical Modeling and Verification of Embedded Systems, <i>P.Eles,</i></p>	<p><b>Decision Diagrams and Synthesis</b> Chair: <i>Marek Perkowski</i></p> <p>Minimization of OPKFDDs Using Genetic Algorithms, <i>M.Jung, G.Lee, S. Park</i></p> <p>An Approach to Minimization of Decision Diagram, <i>P. Kerntopf</i></p> <p>Synthesis of ASM-based Self-Checking Controllers, <i>I.Levin et al.</i></p> <p>Two-criterial</p>	<p><b>Processor Design</b> Chair: <i>Antonio Nunez</i></p> <p>Dynamic Branch Prediction Using Neural Networks, <i>G.Steven et al.</i></p> <p>Applying Caching to Two-Level Adaptive Branch Prediction, <i>C. Egan et al.</i></p> <p>Experimental Evaluation of CPU Performance Features, <i>J.Sosnowski,</i></p>	<p><b>Synthesis and Test</b> Chair: <i>Andrzej Krasniewski</i></p> <p>A HW/SW Codesign Framework based on Distributed DSP Virtual Machines. <i>C. Steger,</i></p> <p>Synthesis of Conditional Behaviours Using Hierarchical Conditional Dependency Graphs and Constraint Logic Programming, <i>K.Kuchcinski, C.Wolinski</i></p>	<p><b>Physical design</b> Chair: <i>Agnieszka Konczykowska</i></p> <p>Timing Driven Wiring on an Advanced Microprocessors, <i>P.Kartschoke, S.Geissler</i></p> <p>Interconnect-driven Short-Circuit Power Modeling, <i>D. Eckerbert et al.</i></p> <p>Transistor Chaining With Integrated Dynamic Folding For 1-D Leaf Cell Synthesis, <i>K.S.Berezowski</i></p>	<p><b>Specialised architectures</b> Chair: <i>Daniel Tabak</i></p> <p>Synchronizing Low-cost Energy Aware Sensors in a Short-range Wireless Cell, <i>M.Nordman</i></p> <p>A Multiple Context Reconfigurable Functional Unit, <i>M.C. Miller, D.Tabak,</i></p> <p>FPGA based controller for heterogeneous Image Processing</p>

		<p>constrain-driven FSM state encoding for low power, <i>M.Koegst et al.</i></p>	<p><i>R.Jurkiewicz, J.Nowicki</i></p> <p>A Comparison of Five Different Multiprocessor SoC Bus Architectures, <i>K.K.Ryu et al.</i></p>	<p>Test Generation and Fault Simulation for Digital Devices based on Cubic Algebra, <i>S.Hyduke et al.</i></p> <p>Self-Testing of user-Programmable FPGAs based on the concept of linear segments, <i>P.Tomaszewicz, M.Rawski</i></p>	<p>A global routing Technique for wave-steering design methodology, <i>N.Funabiki et al.</i></p>	<p>System, <i>M.Gorgon</i></p> <p>FPGA Implementation of Addition as a part of the convolution, <i>E. Jamro, K.Wiatr</i></p> <p>Genetic Algorithm in FPGA Implementation of Addition as a Part of the Convolution <i>E. Jamro, K.Wiatr</i></p>
17.30 18.30	<p><b>DSD Programme Committee Meeting</b> (directly after the last session)</p>					
18.30	<p><b>Welcome Cocktail</b></p>		<p><b>Conference Dinner at 19:00</b></p>			