

Architectural Mapping for Coarse-Grained Heterogeneous Reconfigurable System on Chip

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Thesis Abstract:

As an emerging technology, Digital Radio (or Software Defined Radio) shows promise in terms of improved audio quality, enhanced content delivery and multifunctional platforms. However, there are a number of different standards for Digital Radio, which can vary from country to country and region to region. The reasons for this depend on a number of factors including the cost of moving from conventional analogue transmission and some geographical considerations.

As a consequence, there is a desire to make Software Defined Radio, where the Radio receiver can automatically choose the most suitable (or available) mode of reception and method of content delivery. The high data rates of Digital Radio require very high processing capabilities, and these may not always be best achieved in software. Thus there will be a need to implement some processing in hardware. However, whatever platform is chosen, an Operating System will be required to manage the system resources, especially battery life, through improved efficiency.

This dynamic environment may be harder to control than one which is “ready for anything”, but it can also be more efficient, through design, and therefore more suited to the portable environment where size, weight and battery life are important factors.

We can consider this environment as a heterogeneous system, consisting of different devices, processing elements, interfaces, users, states etc. A Heterogeneous Reconfigurable System on Chip (HRSoC), which has a controlling CPU attached to a reconfigurable fabric or array, allows us to design a Digital Radio receiver in incremental stages which can have dynamic implementation of various functions according to processing need and power restrictions, such as loading an audio decoder module when needed, or switching off a video decoder if no video information (or display) is present. It is also possible to compare the implementation of these tasks in software as well as hardware, and to determine how to optimise the use of available HRSoC resources.

A recent (2005) paper states, “*One of the most challenging tasks in modern System-on-Chip design projects is to map a complex application onto a heterogeneous architecture in adherence to the specified performance and cost requirements*” [1].

I will be investigating the role of the controlling CPU, the Real-Time Operating System (RTOS), the energy, area and control complexity of the reconfigurable array, and how to map the Digital Radio algorithm onto both hardware and software.

The particular Digital Radio algorithm I am investigating is Digital Audio Broadcasting (DAB) Eureka 147. This is of interest because of its high computational complexity, modularity and setup based on user demand and reception environment changes. It is now the standard to be adopted in Australia.

Further research will focus on Network on Chip communication methods, shared-memory, inter-process communication, partitioning of the algorithm in hardware and software, and resource management by the operating system.

Research has shown improvements in energy efficiency and speedup by decoupling data flow and control flow and I will be investigating how this can be exploited in this system. I will also be investigating how tasks can be dynamically migrated, even during partial processing.

From this I hope to achieve outcomes that improve modelling and design methodologies and tools, and assist in efficient runtime control of this flexible computing medium.

1. Kempf, T. et al, *A Modular Simulation Framework for Spatial and Temporal Task Mapping onto Multi-Processor SoC Platforms* in *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE'05)*, 2005