

A High-Performance Computing Module for a Low Earth Orbit Satellite Using Reconfigurable Logic

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Abstract. A hierarchy of FPGAs, DSPs, and a multiprocessing microprocessor provide a layered high performance computing module which will be used to enhance the performance of a low-earth orbit satellite, FedSat-1, which will be operational in 2001. The high performance computer will provide additional hardware redundancy, on-board data processing, data filtering and data compression for science data, as well as allowing experiments in dynamic reconfigurability of satellite computing hardware in space.

1 Introduction

The Co-operative Research Centre for Satellite Systems (CRCSS) is a new research venture distributed over several universities, research labs and industrial partners across Australia, which commenced operations in January 1998 [1]. The mission of the CRCSS is to deliver a new, sustainable advantage for Australian industries and government agencies involved in services based on the applications of future generations of small satellites. Under the Centre's strategy, by focusing on affordable space missions which can be achieved in a relatively short time, Australia will regain experience in designing and operating space assets required for future commercial and public benefit applications. The budget for the Centre totals \$A56 million over seven years, including contributions from government, research and industry participants.

The first major space project for the Centre will be a small, experimental scientific satellite, FedSat-1, to be operating in time to celebrate the Centenary of Federation of the Commonwealth of Australia (2001). The principal missions of FedSat-1 are currently as shown below.

- *Communications:* Ka-band satellite communications; experiments in multi-media data transmission, paging, remote area messaging and location service; relay of scientific data and control, innovative earth station design.
- *Space Science:* NEWMAG experiment in solar-terrestrial physics, to measure electrical currents and perturbations in the Earth's magnetic field.
- *Remote Sensing:* GPS occultation experiment for atmospheric sounding.

- *Engineering Research*: test of solar panel efficiency, new on-board processors, space qualification of GPS receiver.
- *Education and Training*: Researchers, students and engineers will gain experience in space technology and science, will design and test payloads and participate in experiments and research based upon the operation of those payloads.

This paper particularly addresses the design of a new high-performance computing module which incorporates reconfigurable logic.

2 Characteristics of Space Electronics

There are certain obvious characteristics of electronics systems for a typical small, low earth orbit satellite which greatly affect system design choices.

- The satellite operating environment is significantly different from that encountered in terrestrial systems. The near-vacuum conditions reduce convective cooling capability making temperature management more complex. Circuitry and packaging materials must be free from out-gassing (evaporation of volatile materials in vacuum).
- The lack of atmospheric protection increases the incident radiation which can produce soft and hard circuit faults.
- The circuitry undergoes extreme acoustic and mechanical vibration during launch.
- Hardware faults cannot be repaired, requiring high-reliability manufacture, assembly and operating techniques. Backup systems are needed for mission-critical sub-systems.
- Faults are difficult to diagnose due to limited observability of system components.
- For a small satellite reliant on photovoltaic power generation, total power is very limited. For our 0.125m^3 satellite, only a 0.25m^2 surface area is presented to the sun. Overall, this provides only about a 10W average available power for all satellite services, payloads and communications.
- Our satellite has a total mass budget of 50 kg, of which only about 1/3 is available for payloads. Hence light, compact circuitry is preferred.
- Low earth orbit satellites might typically only be visible from a given Tracking, Telemetry and Control ground station for four to six passes of 10 minutes each per day. The availability of bandwidth for downloading telemetry data and uploading control information is limited.

Because of the unusual operating conditions, and the need for reliability, satellite electronics have typically used a very conservative design approach [2]. Specialised packaging and assembly techniques are used. Often, individual components for critical sub-systems must be specially space-qualified. Every subsystem of a planned satellite is typically tested in an environmental chamber to confirm its space-readiness. This conservative design approach is naturally in opposition to conventional computer design, which has very short product lifetimes and rapid adoption of the latest components.

3 Aims of the High Performance Computing Program

In order to further the mission of the CRC for Satellite Systems, the following aims have been developed for a High Performance Computing research project:

- To evaluate improvements in satellite performance enabled by the use of high performance computing technologies in space and on the ground.
- To develop computer architectures and algorithms for use in satellite systems which take advantage of reconfigurable computing technologies.

Our approach for achieving these aims is to develop a HPC architecture suitable for satellite use, evaluate performance gains through ground-based experiments across a range of satellite scenarios, and gain experience and mission-specific results through flying a HPC module onboard FedSat-1. We have therefore identified the following objectives for a FedSat-1 payload:

- To provide high performance processing onboard FedSat-1 - utilizing a combination of processors and reconfigurable logic - capable of implementing data compression, data filtering, communications baseband processing, message storage, and inter-experiment data computation.
- To conduct experiments on the practicalities associated with reconfiguration (including partial or dynamic reconfiguration) of hardware in space and to evaluate improvements in satellite performance offered by this approach.

The remainder of this paper investigates some details of how these aims might be achieved.

4 A Conventional On-Board Computer for a Small Satellite

Typically, on-board computers for satellites have been very conservatively designed [3]. Even recent small satellites might contain only an Intel 186 processor with 1 MByte memory. However, there has recently been a trend to incorporate extra intelligence in satellites, to perform mission activities more independently of ground control.

A typical, modern, small satellite would contain a modular data processing system which can be customised for a particular mission with selections from a range of individual cards or modules. Such a system might consist of the following modules:

- *Central Processing Unit*, which coordinates all the activities of the satellite, and deals with commands for core satellite activities such as attitude control, power management and health monitoring.
- *Redundant Processing Unit*, which is a backup processor for the CPU to increase system reliability. It might be an identical CPU module, or it may be a smaller, less powerful module which can still maintain a minimum of computing services.
- *Data Acquisition Unit*, which interfaces with the data streams to and from the payloads. Data from analog or digital interfaces is converted into data packets for transmission to the ground-station. Control packets are converted into appropriate

analog or digital control signals. Multiple modules may be needed to cope with a large number of different interfaces.

- *Mass Memory Unit*, which contains high-density solid-state mass memory for storage of remote sensing data awaiting transmission to ground.
- *Data Packet Handler*, which deals with the transmission of data packets to and from the controlling ground-station via the communications sub-system and routes these packets to the DAU or CPU as required.

For a small satellite, the on-board computer is typically in the range of 2-5kg in mass and 5 W power dissipation. This represents a substantial proportion of the total system mass and power budgets.

5 Design of a New High Performance Computing Module

In order to meet the aims of our research program, we are currently designing a new High Performance Computing card which would fit into the modular computing framework of our satellite, and service the high performance computing needs of the satellite payloads. The system design constraints of limited mass, volume and power, need for reliability and redundancy, and short design time have led to the following preliminary design decisions.

Firstly, a central processor running a multiprocessing operating system will provide access to other computing modules such as Data Acquisition or Mass Memory units via the system backplane. To increase overall system reliability, this processor will have the capability to take over control from the CPU in the event of failure of the main processor card. Otherwise, this processor will be available to provide enhanced system computing capability.

Secondly, a DSP chip will be used to provide dedicated real-time data processing for payloads, such as data processing, data filtering, or data compression. A key selection criterion here will be power consumption per MIP.

Thirdly, dynamically reconfigurable FPGAs will be used to provide a flexible data interface to payloads. High speed data streams will be able to be handled in real-time, with preliminary data processing and formatting implemented in hardware.

Software applications for the DSP subsystem, and programmable hardware configurations for the FPGA subsystem will be able to be uploaded to the satellite during the lifetime of the mission, to allow additional system flexibility.

At this stage, the tentative list of experiments which might use the High Performance Computing module includes the following:

- Digital filtering and modulation/demodulation of communications waveforms.
- Communications system error detection, correction and monitoring.
- Adaptive high-speed communications protocols.
- Data encryption and decryption.
- Data compression for remote sensing data.
- Position estimation for the satellite.
- Position estimation for mobile terrestrial transmitters.
- Emergency replacement of main platform computer, or other system components.

- Store and forward packet switching functions for low bandwidth remote-area communications.
- In-flight system reconfiguration via uplink communications channel.

6 Conclusions

The expected outcomes of the High Performance Computing project are improved satellite system performance across many different metrics:

- *Reliability*: Increased system flexibility to cope with individual component failures.
- *Flexibility*: Ability to deal with many different payload interfaces, increased flexibility for post-launch system upgrades, ability to reconfigure hardware support during different mission phases.
- *On-board Data Processing*: Ability to deal with real-time high speed data streams in a power efficient manner.
- *Received Data Throughput*: Increased amount of useful payload data transmitted to earth through data filtering (data analysed to send most useful samples), data compression, and adaptive communications channel coding (to make best use of available downlink bandwidth).
- *Design Time*: Reprogrammable logic allows late system changes to overcome problems encountered during system integration and test.
- *Power Optimisation*: Computations can be assigned to reprogrammable hardware or DSP software to optimise power consumption.
- *Mission Lifetime*: Flexible hardware configurations and interconnections can be used to make best use of available satellite resources throughout mission lifetime.

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