

# Digitally-Implemented Naturally Sampled PWM Suitable for Multilevel Converter Control

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**Abstract**—For dynamic closed loop control of a multilevel converter with a low pulse number (ratio of switching frequency to synthesized fundamental), natural sampled pulse-width modulation (PWM) is the best form of modulation. Natural sampling does not introduce distortion or a delayed response to the modulating signal. However previous natural sampled PWM implementations have generally been analog. For a modular multilevel converter, a digital implementation has advantages of accuracy and flexibility. Re-sampled uniform PWM is a novel digital modulation technique which approaches the performance of natural PWM. Both hardware and software implementations for a five level multilevel converter phase are presented, demonstrating the improvement over uniform PWM.

**Index Terms**—Modulation, modulator bandwidth, multilevel converter, natural PWM, re-sampled uniform, re-sampling, uniform PWM.

## I. INTRODUCTION

CARRIER-based pulse-width modulation (PWM) schemes can be broadly broken into two categories, natural sampled and uniform sampled (see Fig. 1).

### A. Natural and Uniform Sampled Pulse Width Modulation

Uniform sampled and space vector PWM are sampled data systems. They sample the signal input at the beginning of the switch cycle, before the actual switching edge reflects this value later in the cycle. This delay in response is significant when the ratio of modulating frequency to carrier frequency (the pulse number inverse,  $f_1/f_c = 1/N$ ) approaches and exceeds unity. It leads to a frequency response roll-off which obeys a Bessel function, similar to the familiar sinc function roll-off for pulse amplitude modulation (PAM) (see Fig. 2). Another unwanted effect of uniform PWM is odd harmonic distortion of the synthesized waveform. The severity of these effects is a function of the ratio of the modulating and carrier frequencies,  $f_1/f_c$ . This ratio may approach and pass unity in high power active filters (high  $f_1$ , low  $f_c$ ), by which point these effects have become significant and limiting [1], [2].

Naturally sampled PWM is traditionally an analog technique where the input signal is naturally sampled by the carrier triangle waveform at the instant of the switching edge. Naturally sampled PWM can react instantly to changes in input signal and

produces no attenuation or distortion of the synthesized waveform. However as the ratio  $f_1/f_c$  rises for a given modulation depth  $M$ , the slew rate of  $f_1$  will exceed that of the carrier triangle and an extra pulse will be generated. If these additional pulses can be tolerated, the integrity of the synthesized waveform is preserved [1], [2].

In summary, for a high power, low switch frequency converter—especially a multilevel converter—a naturally sampled PWM modulator offers the most promise for wide bandwidth, low delay and low distortion [3]. This paper examines a method of implementing natural sampling using digital rather than analog techniques.

### B. Multilevel Carrier-Based PWM Generation

Many multilevel converter implementations published in the literature demonstrate their modulation technique using natural sampled carrier based diagrams. Usually no explanation is given as to why this particular method is chosen. It is assumed that clarity of explanation and understanding, or simplicity of implementation are two major reasons; rarely is the actual reasoning justified or explained.

Natural sampled PWM is invariably implemented as an analog technique. An analog technique does not lend itself to a high power multilevel implementation. Consider a multilevel converter consisting of a number of three level full bridge modules, such as suggested by Hammond [4] and Peng and Lai [5]. A digital implementation would be preferred because of the following.

- Switching instants are crystal accurate, at least at the signal level. It is possible to compensate for the switching delays in the power stages. More importantly, the switching instants are repeatable from module to module. This ensures good cancellation of the switching frequency terms in the combined multilevel output.
- A digital microcontroller based implementation can be interrogated, tuned, even reconfigured more easily than an analog one. These changes could be made online, and again, would be consistent from module to module.
- A digital system can be distributed master slave style more easily than an analog implementation, which is an advantage for a modular approach. Digital signals are more easily shared among isolated modules.
- Digital signals are more immune to noise than analog signals in a noisy high power environment.

This is the motivation for seeking to create a digital implementation of naturally sampled PWM.

To retain the versatility of the traditional analog implementation, the digital implementation should accept an arbitrary real

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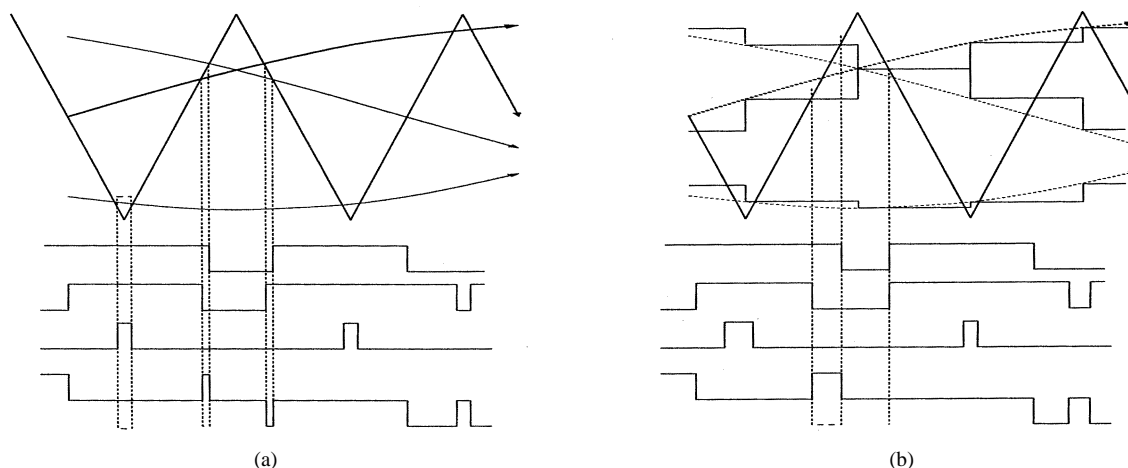


Fig. 1. (a) Natural sampling versus (b) uniform sampling. Note the delay introduced by uniform sampling.

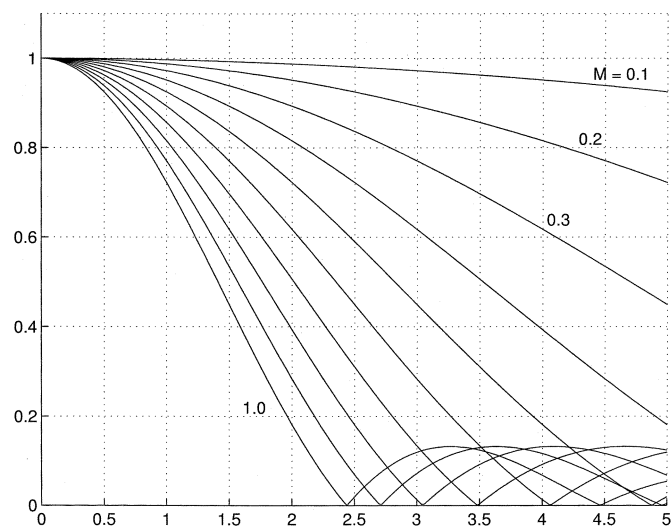


Fig. 2. Transfer function (versus the ratio  $f_1/f_c$ ) of a uniform PWM modulator. For uniform modulation, the attenuation is a function of both modulation depth  $M$  and the ratio of modulating signal frequency to carrier (switch) frequency ( $f_1/f_c$ ).

time input signal. Such signals will occur when the modulator is in the feedback loop of a closed loop system, or part of an active filter. The combined modulator and converter should still be able to be modeled as a linear wideband amplifier [3].

The re-sampling technique allows fast control loops to benefit large, low switching frequency converters. For example, Tzou [6] has implemented a fully digital controller for dc-ac inversion using a DSP. The sampling rate of the current loop is 15.36 kHz ( $256 * 50$  Hz), and the switching frequency is twice this, as the converter is a small UPS. A larger multilevel converter with a switching frequency many times lower could still use this high sample rate to advantage to achieve similar results using digital natural PWM.

### C. Space Vector Versus Carrier Modulation

It is of note that the distinction of carrier based modulation versus space vector modulation is a separate issue to that of natural versus uniform sampling. In a three phase converter, carrier based modulation allocates the pulse width of each phase leg

independently based on three independent desired phase voltages. Space vector modulation allocates the pulse widths of each inverter leg by examination of the desired three phase voltage vector in a two dimensional space. The extra degree of freedom (the zero-sequence component) is then used to centre the three switching instants in the switch period, or move them to one end to create a discontinuous switching algorithm. This allocation of switching times in the transformed space and the resulting extra degree of freedom is the only difference between these two techniques [7]. It is possible to create carrier based modulators which, with the correct addition of zero sequence component, matches any desired space vector generated modulation, and a “naturally sampled analogue space vector modulator” [8].

The digital implementation of naturally sampled PWM presented in this paper is demonstrated for a single phase leg using sine-triangle carrier based techniques. It may be extended to three phase converters trivially using three appropriately phased modulating waveforms. Although not pursued here, the techniques should also be equally applicable to space-vector modulation, although the implementation will be nontrivial.

## II. RE-SAMPLED UNIFORM

The approach to generating a digital implementation of natural sampling presented here is most accurately described as re-sampled uniform. The switch frequency of a large converter is often limited by its semiconductor switching devices, particularly for GTOs. This is despite the capability of modern micro-controllers and DSPs to sample and process control signals at a far higher rate. With re-sampled uniform, although the same switching/carrier frequency  $f_c$  is used, an attempt is made to retain the wider bandwidth gained as a result of using a higher sampling frequency  $f_s$ . Samples are taken more frequently than once per switching edge at the beginning of the PWM switch period. This is most easily achieved by sampling at an integer multiple of the switching frequency. This ratio will be referred to as the re-sampling ratio,  $rsr = f_s/2f_c$ . Note that this is the number of samples per switch edge, rather than per pulse; hence the factor of two.

Uniform sampling already comes in two variants—symmetric, where the sample is held for the complete carrier period

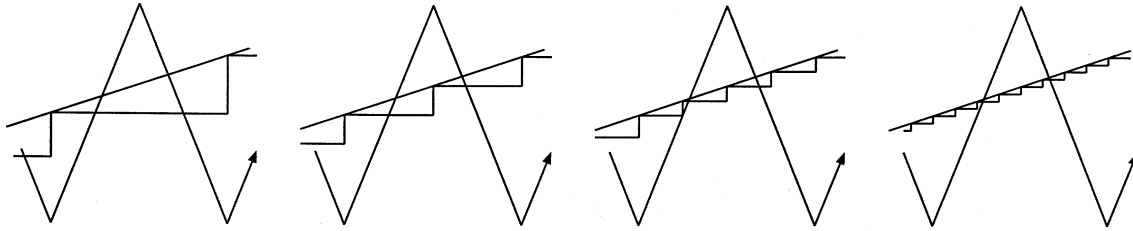


Fig. 3. From left to right, the existing techniques of symmetric and asymmetric uniform sampling; and an extension of the concept, re-sampled uniform sampling with re-sampling ratios (rsr) of 2 and 4.

( $rsr = 1/2$ ); and asymmetric, where a second sample is taken halfway through the carrier period for the second switch edge ( $rsr = 1$ ). Asymmetric uniform sampling is the preferred method, since each switching edge is the result of a new sample and leads to better performance [9]. For both of these cases, the reference is held constant throughout the switch period.

However, for a re-sampling ratio greater than one, one or more of the samples will occur part way through the switch sub-period (Fig. 3). If according to a mid switch period sample, the PWM edge is still to occur, then its position is recalculated based on this more recent sample [Fig. 4(A)]. This algorithm will react to transients at the sampling rate rather than at the switching rate and so exhibit lower delay and wider bandwidth. On average, the group delay of the input signal is now  $1/2f_s$  rather than  $1/2f_c$ .

Two problems complicate the implementation of this technique. The first is the possibility of missed edges. When the modulating waveform is varying rapidly, it is possible that based on the previous sample, the PWM edge is yet to come; however based on the current sample, the edge should have already occurred. The best solution is to force the edge to occur immediately [Fig. 4(B)]. As shown in the figure, 'immediately' may not necessarily mean at the sampling instant, if some computation delay must be allowed for in a software implementation.

The second problem is the possibility of generating more than one edge per switching cycle. This happens when multiple intersections of the samples and the triangular carrier occur, either erroneously, because of the stepped nature of the sampled waveform [Fig. 4(C)], or quite legitimately—true natural sampling would have done the same [Fig. 4(D)].

Here, the problem of multiple edges is handled according to what is most expedient to the implementation. In the microcontroller software solution, only the first calculated switching edge is accepted in each switch cycle. Any subsequent edges are simply ignored. In the hardware approach, any edge is accepted, although it would be an easy matter to latch only the first edge and reject subsequent edges until the end of the switch cycle.

### III. RE-SAMPLED UNIFORM SOFTWARE IMPLEMENTATION

#### A. Microcontroller Software Implementation

The design of many microcontroller timer and PWM peripherals complicates or even prevents the implementation of re-sampled uniform PWM. Double buffering and first-in, first-out (FIFO) buffers, usually considered a feature, prevent the reloading of the pulse width value. In these situations, the software must calculate and decide whether the edge will occur in the current sample period, and only *then* load the edge

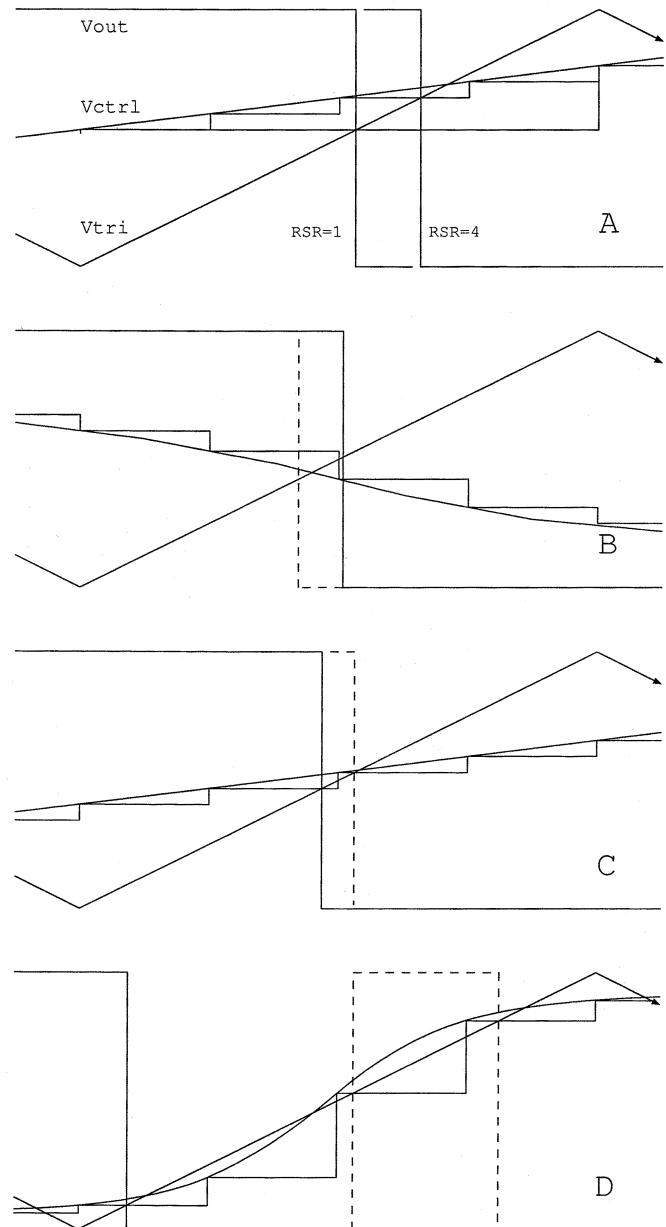


Fig. 4. Re-sampled Uniform PWM—by re-sampling the input *during* the switch cycle instead of only at the beginning, a more accurate switching edge position can be calculated (A). However it is now possible to miss an edge (B) or generate multiple edges (C&D).

command and time. Further, an equality comparison between the pulse width value and the timer (rather than a greater-than comparison) also requires the software to ensure edges are not

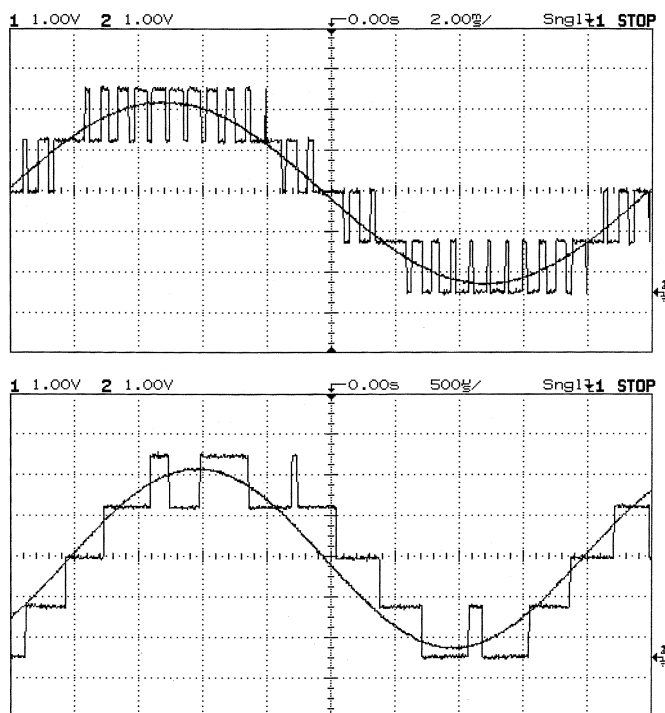


Fig. 5. 80C196 generated five level waveform,  $f_c = 450$  Hz,  $f_1 = 50$  Hz (top) and 250 Hz (bottom). In both cases,  $M = 0.9$ , and the re-sampling ratio = 4 ( $f_s = 3600$  Hz).

missed. These complications incur a considerable software overhead and limit the useful possible re-sampling ratio.

This re-sampled technique was implemented on the Intel 80C196KB microcontroller. The internal 10-b analog to digital converter (ADC) samples the analog generated modulating waveform. Within the “conversion finished” interrupt routine, this sample is compared to (subtracted from) four phase shifted triangular carrier waveforms. The software determines if any edges should occur before the next sample. If so, these are loaded into the timer module, which will automatically generate them before the next ADC interrupt. To allow for this computational overhead, a delay between sampling and loading edges must be introduced. This delay was reduced to a fixed  $44 \mu\text{s}$  for this five level (four output) modulator. This delay, along with the ADC conversion time, limits the useful re-sampling period and hence re-sampling ratio for a given switching frequency for this processor.

The Motorola MC68332 microcontroller is an example of a more suitable choice for a microcontroller implementation of re-sampled uniform. This has an intelligent timer peripheral (TPU) which removes much of the computational overhead. The PWM comparison is a greater-than comparison and pulse width values may be reloaded part way through a PWM cycle. The TPU also has 16 output pins which lends it to multilevel control.

### B. Microcontroller Software Implementation Results

Figs. 5–7 were collected from the five level 80C196 microcontroller implementation, operating with a carrier frequency of 450 Hz. The five level waveforms were created by the summation of four two level PWM waveforms at the logic level. The gain of the modulator as implemented is  $1V/V$ .

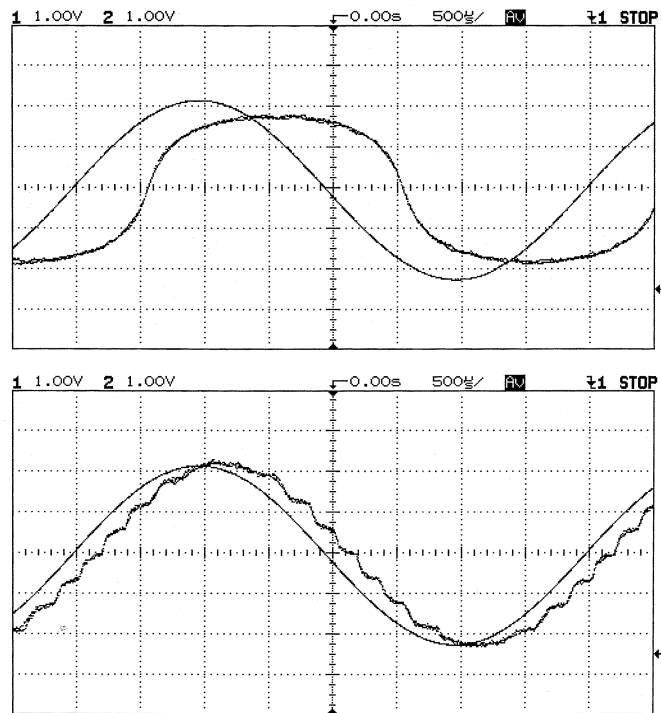


Fig. 6. 80C196 re-sampled uniform.  $f_c = 450$  Hz,  $f_1 = 250$  Hz and  $M = 0.9$ . Uniform asymmetric sampling (re-sampling ratio = 1) (top) produces significant odd harmonic distortion, but digital natural (re-sampling ratio = 4) (bottom) makes a large difference. (Averaged 64 times by the oscilloscope).

A small scale laboratory five level flying capacitor converter was constructed and successfully controlled by the gate array hardware modulator discussed in the following section. However, the results of the modulator alone are shown in this and the following section so as not to obscure the results of the re-sampling technique.

Fig. 5 shows 50 Hz and 250 Hz sine waves of modulation depth  $M = 0.9$  and the resulting five level waveforms. Although the synthesized fundamental frequency  $f_1 = 250$  Hz is a significant fraction of the carrier and hence switch frequency  $f_c = 450$  Hz, a five level converter can produce a good approximation of the original. Note that both of these waveforms were produced with an oversampling ratio of four.

The attenuation, distortion and delay inherent in uniform sampled PWM, and then the improvement which can be achieved through re-sampling, is shown in Fig. 6.

These smoothed waveforms are the multilevel PWM output waveforms averaged by the oscilloscope. Because the PWM modulator was clocked from a crystal oscillator and not phase locked to the modulating signal as it should be for truly synchronous PWM, the PWM waveform slowly slipped with respect to the modulating waveform. This allowed the oscilloscope, triggered from the modulating waveform, to be used to average the PWM waveform over 64 successive triggers. Using the oscilloscope to average the waveforms in this way introduces no filtering phase distortions.

In Fig. 6, the modulating waveform is a 250 Hz sine wave, with modulation index 0.9, and the carrier frequency is again 450 Hz.

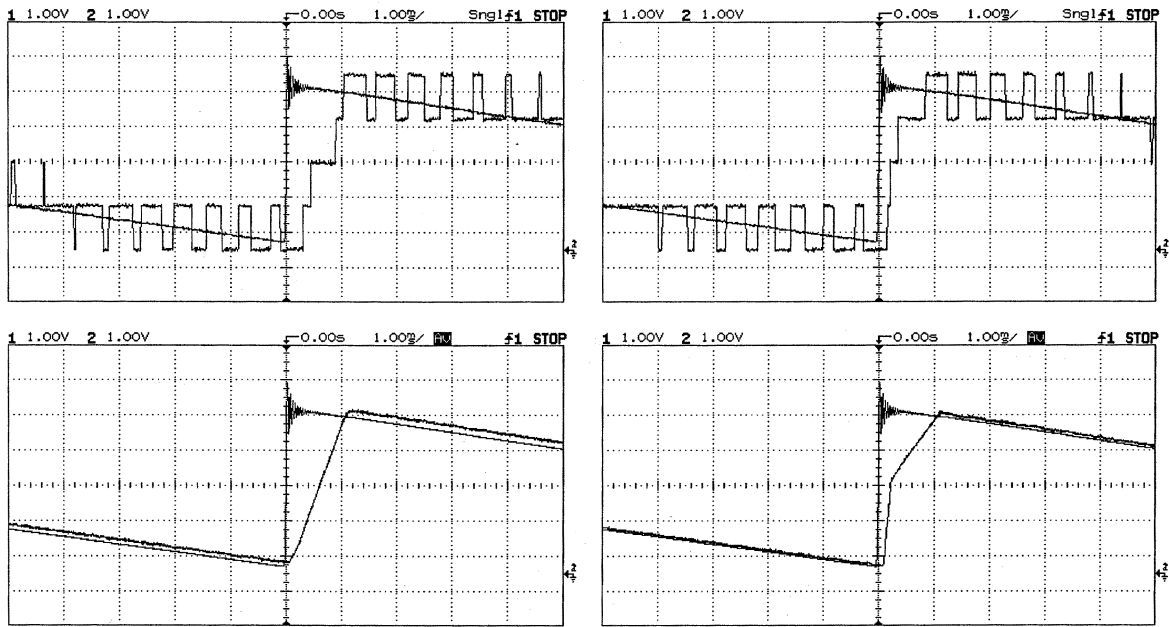


Fig. 7. 80C196 re-sampled uniform. Re-sampling ratio = 1 (left) and 4 (right). (Below—Averaged 64 times by the oscilloscope).

The upper plot is asymmetric uniform sampling. The converter samples at twice the switching frequency, 900 Hz, and this leads to the average phase delay seen in the fundamental of approximately  $600 \mu\text{s}$  ( $T_s/2$ ). The odd harmonic distortion of the modulating waveform attributable to uniform sampling is clearly visible.

The second plot shows a re-sampling ratio of four ( $f_s = 3.6 \text{ kHz}$ ) can reduce both delay and distortion. The apparent delay of  $200 \mu\text{s}$  can be accounted for as  $20 \mu\text{s}$  for a/d conversion,  $44 \mu\text{s}$  of delay deliberately introduced in the calculation of the edge times to allow for computation time, and the average delay due to the sampling process of  $140 \mu\text{s}$  ( $T_s/2$ ). The distortion is greatly reduced, but more interestingly, changes in character. For simple uniform sampled, the distortion component is predominantly third harmonic, the same as for two-level uniform sampled. The frequency of the distortion component of the re-sampled uniform waveform is roughly 15 times  $f_1$ .

The response to the sawtooth waveform shows the reduced delay, and hence following error, and improved transient response due to re-sampling (Fig. 7). The kink in the transient response is due to software latches (flags) which enforce only one pulse per period. This was necessary due to the risk of overflowing the (six deep) 80C196 timer FIFO. This demonstrates that strictly enforcing the switching frequency only compromises the large signal transient response, or more correctly, the large signal slew rate.

#### IV. RE-SAMPLED UNIFORM HARDWARE IMPLEMENTATION

##### A. Gate Array Implementation

The second approach documented here was a hardware implementation using a field programmable gate array (FPGA)—the Altera FLEX series of SRAM based programmable logic.

A three phase, five level (12 output) modulator was implemented in an Altera FLEX 8820, initially with 7-b resolution,

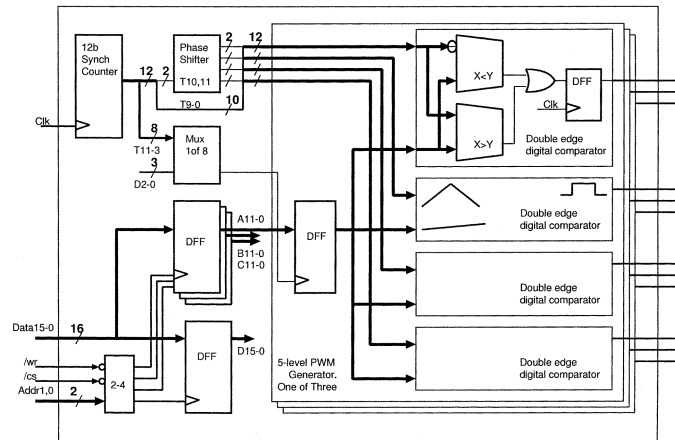


Fig. 8. Block diagram of the programmable gate array implementation of re-sampled uniform.

which was then extended to 11-b resolution (Fig. 8). The DSP interface to this PWM peripheral was through four 16-b memory mapped registers, three for each of the PWM phase inputs, and the fourth for configuration. A tap from the timer chain updated (latched) the new data to the comparators synchronously. This tap position was programmable to enable different re-sampling ratios to be evaluated. Similar circuitry (not shown) generated the trigger signal for the ADC and subsequent DSP interrupt. Programmable dead time (also omitted) was later implemented for each switch pair. A full set of circuits for the seven bit implementation can be found in the author's doctoral thesis [2].

The FPGA was part of a DSP (the TMS320C31) based controller board. As well as the FPGA, other key components were external RAM and boot EPROM, a serial port, four 12-b analog to digital converters and a quad 8-b digital to analog converter.

Leading or trailing single edge pulse width modulation can be easily generated digitally with an up or down counter, and a digital comparator. Double edge modulation has previously been

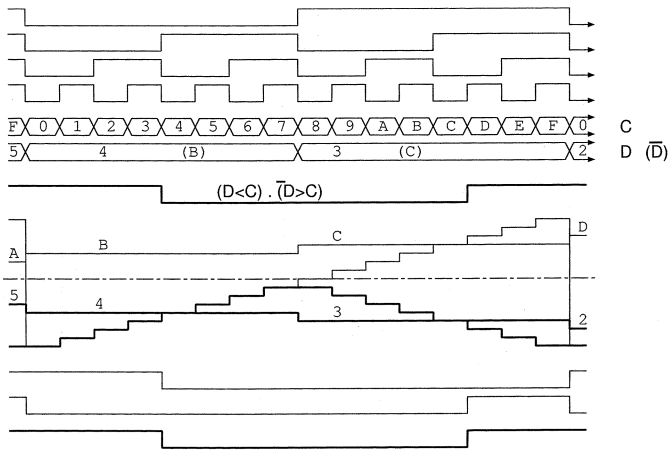


Fig. 9. Operation of the programmable gate array implementation of re-sampled uniform. A four bit counter value (C) is compared with a three bit modulating value (D) and its complement ( $\bar{D}$ ) to create PWM with three bit resolution. Two separate comparators implement double edge PWM, one generates the leading edge, the second the trailing edge.

implemented with up-down counters. For this multilevel implementation, a novel technique has avoided the need for multiple, synchronized up-down counters. All the phase shifted double edge PWM outputs are generated from a single up counter reference (Fig. 9).

Double edge PWM can be generated with a sawtooth carrier if the leading and trailing edges are generated by two separate comparators. A sawtooth rather than a triangular carrier only requires a unidirectional counter rather than the more complex up-down counter. This sawtooth carrier can then be phase shifted trivially by simply manipulating the most significant bits.

Because the two comparators are created using combinatorial logic, many of the terms are common to both and so they do not consume many more resources than a single comparator would. An up-down counter however is generally more complex and resource hungry. The one counter is common to all modulation and carrier phases, which ensures that the entire modulator is synchronized at all times.

### B. Gate Array Implementation Results

For the evaluation of this system, the PWM modulator was again configured simply as a linear amplifier with a gain of  $1V/V$ , just as the micro-controller implementation had been. The timer within the FPGA was responsible for initiating a 12-b AD conversion at a selectable sample rate  $f_s$ . Upon completion, the DSP was interrupted, fetched the ADC result, scaled it, and then wrote the result to the PWM peripheral implemented with the FPGA. The FPGA timer subsequently synchronously loaded an internal PWM register to ensure a fixed delay between AD sample and PWM output. The four logic level outputs of a single phase were buffered and resistively summed to give a multilevel output.

A Tektronix 2630 spectrum analyzer was used to provide the stimulus and to evaluate the transfer function of the modulator. The stimulus was a repeating 0 to 2 kHz or 5 kHz swept sine wave “chirp.” The spectrum analyzer calculates the transfer

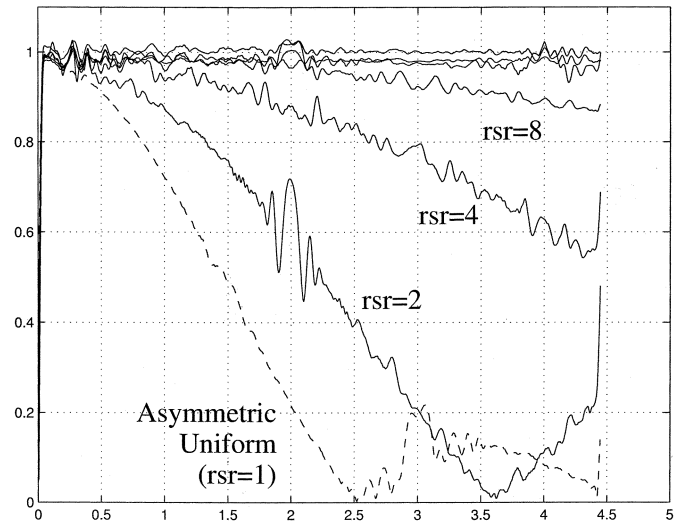


Fig. 10. Transfer functions for different re-sampling ratios are shown for the Flex digital natural implementation for modulation depth  $M = 1.0$ , plotted against  $1/N = f_1/f_c$ . The transfer function of the previously analyzed 80C196 based uniform modulator (conventional asymmetric uniform sampling) is shown dashed for comparison.

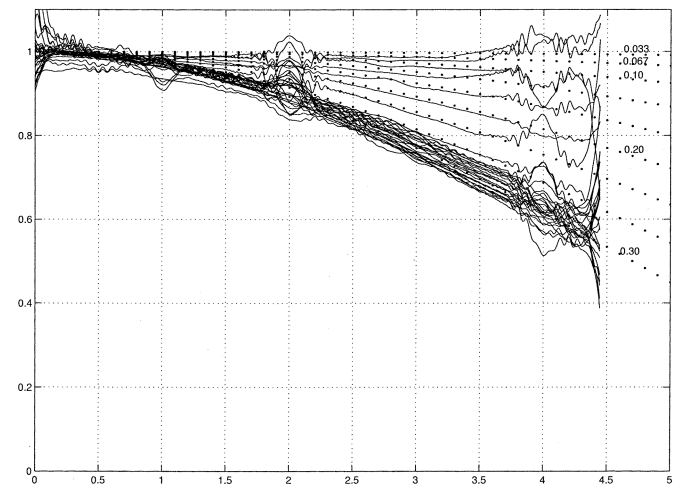
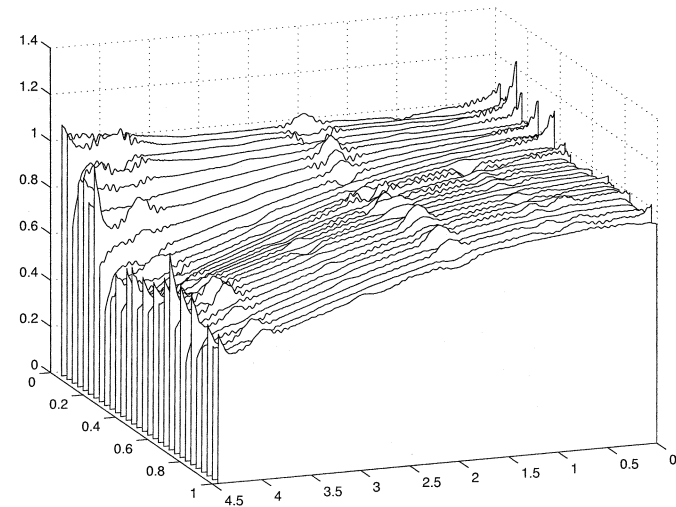


Fig. 11. Three-dimensional waterfall plots show the transfer function of the re-sampled uniform modulator (DSP-Flex) plotted against frequency ( $0 < f_1/f_c < 5$ ) for different modulation depths ( $0 < M < 1$ ). These are for a re-sampling ratio of four.

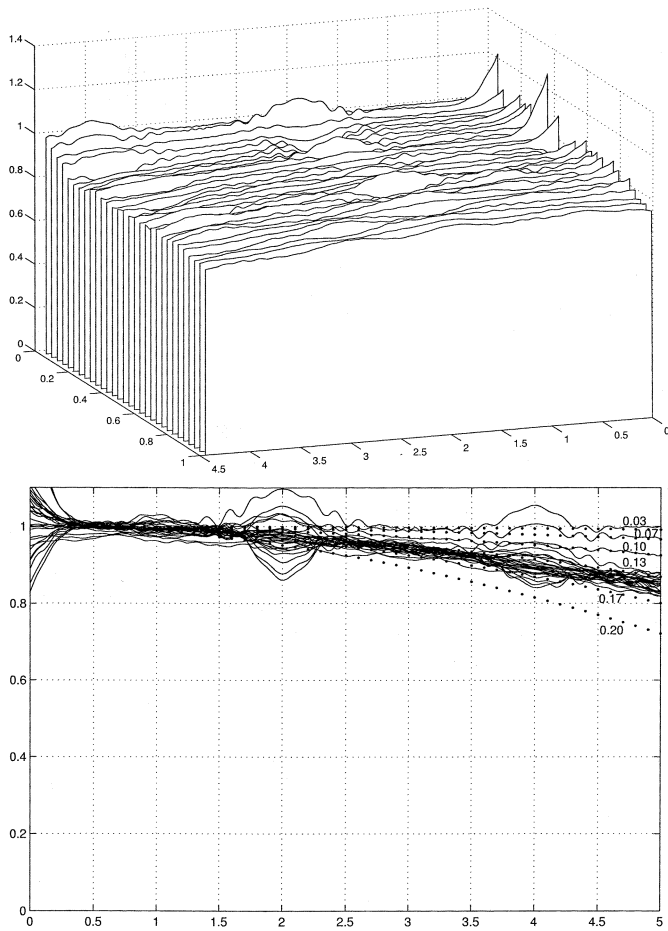


Fig. 12. Transfer function for differing modulation depths as before, but for a re-sampling ratio of eight.

function based on the ratio of the corresponding frequency components in the FFTs of the input and output waveforms. The transfer function of this modulator was captured and plotted for a number of re-sampling ratios for the modulation depth  $M = 1.0$  (Fig. 10).

1) *Bandwidth Improvement Versus Resampling Ratio:* Using re-sampling is seen to improve the frequency response of the modulator, producing a family of curves similar to those produced for uniform modulation for different modulation depths (compare Fig. 10 to Fig. 2). As expected, less roll-off occurs for larger re-sampling ratios. Specifically, Fig. 10 shows that every doubling of the re-sampling ratio is equivalent to the improvement in bandwidth that occurs when the modulation depth is halved for asymmetric uniform sampling.

2) *Bandwidth Versus Modulation Depth:* It was also expected that there would be less roll-off for lower modulation depths for a given re-sampling ratio, as was the case for uniform sampling. To test this, a family of 30 transfer function curves was gathered for this DSP-Flex modulator. The modulation depth was varied from 0.033 to 1.0 while the re-sampling ratio was held constant, first at four, then eight. It can be seen from the plots (Figs. 11 and 12) that the transfer function is relatively independent of modulation depth until the modulating signal's amplitude falls below  $1/\text{rsr}$ .

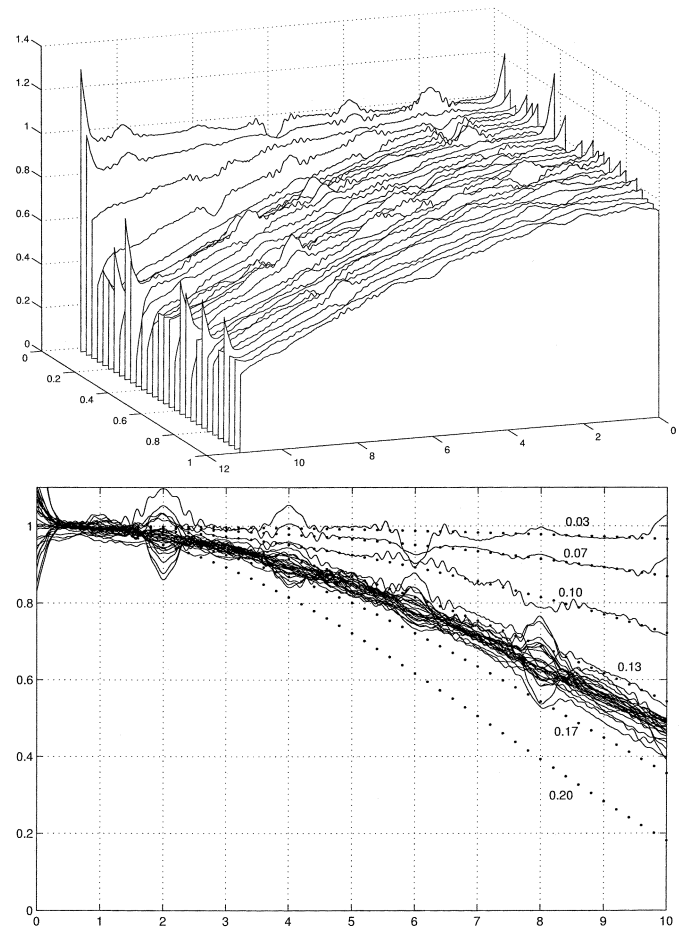


Fig. 13. Transfer function for differing modulation depths, re-sampling ratio of eight (as above). However, note the different x-axis scale for  $1/N$ .

At this point the roll-off improves for smaller values of  $M$ . The attenuation curves then closely match the uniform sampled case.

However the group delay of the re-sampled modulator is greatly reduced compared to conventional asymmetric uniform sampling (Fig. 13).

Some qualitative understanding of this behavior is gained by graphically examining the process of re-sampling (Fig. 14). The choice of an odd number of carriers assists this examination, since for the smallest modulation depths, the modulating signal is effectively interacting with a single carrier of a higher frequency—a familiar problem.

For this example, consider a six level (five carrier) converter which re-samples a modulating sinusoid  $M = 0.2$  five times during one edge period ( $\text{rsr} = 5$ ). This can be seen to be equivalent to a single asymmetric uniform converter with a maximum output amplitude of only one fifth of the multilevel converter, a modulation depth  $M = 1.0$ , and a switch frequency five times that of the multilevel converter.

For modulation depths below this value, the bandwidth of the converter will improve as it does for a single uniform sampled converter. For modulation depths above this value, the transfer function will remain roughly fixed, oscillating around this transfer function.

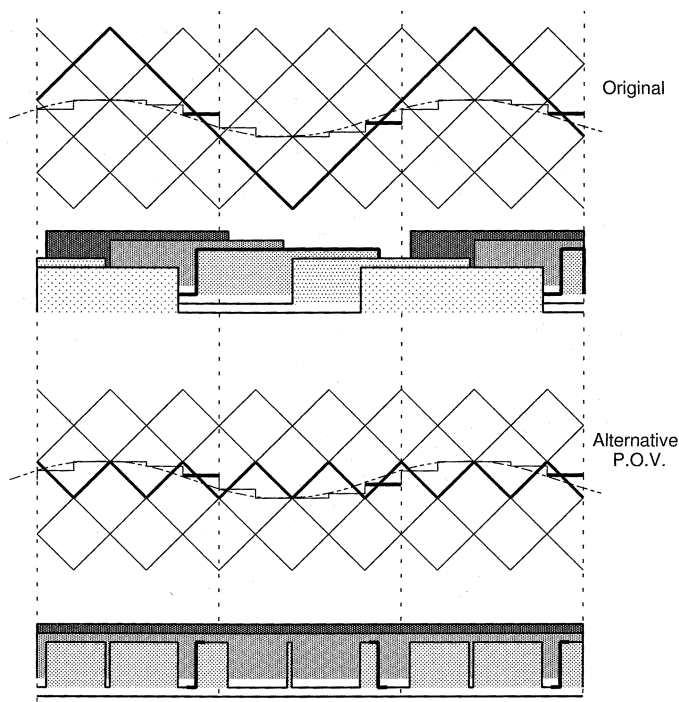


Fig. 14. Alternative point of view of the creation of the multilevel waveform, suggests an alternative derivation of the mathematical description of the multilevel PWM waveform.

In principle, a hardware implementation of re-sampled uniform can operate at a very high re-sampling ratio. The transfer function will then approach that of natural sampling. In practice, the limit will most likely be set by the sampling rate of the control loops.

## V. CONCLUSION

Natural sampled PWM is the best choice for applications which require closed loop, wide bandwidth modulation such as active power filtering. It does not attenuate or distort the modulating signal, even when the frequency of that signal is similar to the switch frequency. Carrier based PWM is also easily adapted to multilevel converter modulation by phase shifting the carriers.

A digital implementation is preferred for multilevel modulation. Switching edges with crystal accuracy and more importantly repeatability are needed to give the best carrier cancel-

lation in a multilevel converter. Digital control is more easily modularized and is more noise immune.

Re-sampled uniform PWM is a digital implementation which approaches the frequency and transient response of natural PWM. Both hardware and software multilevel implementations are presented and the improvement over uniform PWM is demonstrated.

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