

DIGITAL PWM WAVEFORM GENERATION USING ADDERS, NOT COUNTERS.

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Abstract

An alternative approach to digital PWM generation using an adder rather than a counter is presented. This offers several advantages. The resolution and gain of the pulse width modulator remain constant regardless of the module clock frequency and PWM output frequency. The PWM resolution also becomes fixed at the register width. Even at high PWM frequencies, the resolution remains high when averaged over a number of PWM cycles. An inherent dithering of the PWM waveform introduced over successive cycles blurs the switching spectra without distorting the modulating waveform. The technique also lends itself to easily generating several phase shifted PWM waveforms suitable for multilevel converter modulation.

1. INTRODUCTION

The traditional method of digitally generating pulse width modulation (PWM) waveforms involves a binary counter and comparator. Simultaneously generating a high PWM switching frequency with high resolution requires high clock frequencies. For example, generating a 200kHz 8bit PWM signal requires a 50MHz clock. A low clock frequency also gives limited PWM frequency resolution.

This paper presents an alternative approach to digital PWM generation using an adder rather than a counter. In a counter implementation, the sawtooth carrier waveform has a constant slope of one count per clock cycle, and a maximum amplitude which varies with carrier period. In the proposed adder implementation based on Direct Digital Synthesis hardware, the carrier amplitude, hence resolution and gain of the pulse width modulator remain constant regardless of the module clock frequency and PWM output frequency.

The traditional approach along with some of its shortcomings is explained in the next section. The new technique of PWM generation using an adder is presented in section three, with simulation results in the following section.

2. PWM GENERATION USING COUNTERS

The traditional method of digitally generating pulse width modulation (PWM) waveforms involves a digital (binary) counter and comparator. The ATmega8 Atmel AVR series microcontroller's 16 bit timer peripheral is used as an example (fig.1) [1]. The 16 bit timer counter TCNTn is clocked by the system clock or a prescaled submultiple, counting initially up from 0x0000h. As it equals a

fixed or variable period (TOP value), the counter is either reset, producing a sawtooth wave, or changed to down counting, producing a triangular wave.

A separate 16 bit register PWM duty value OCRn is compared for equality each clock cycle. On a match, an output pin can be set high (or low). The pin is subsequently reset low (or high) when the counter reaches 0. Both the PWM period and duty can be changed readily on a cycle by cycle basis so creating quite complex waveforms if desired (see fig.2)

Figure 32. 16-bit Timer/Counter Block Diagram⁽¹⁾

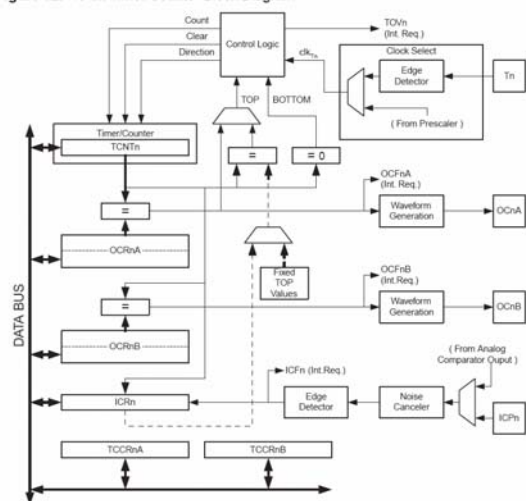


Fig. 1 An example of a typical 16 bit timer peripheral from an Atmel AVR microcontroller, the ATmega8 [1]. PWM waveforms are generated by comparing the timer value TCNTn with register OCRnA or OCRnB. The timer period is set by the TOP and BOTTOM logic signals driven by matches with the period register IORn.

Figure 39. Phase Correct PWM Mode, Timing Diagram

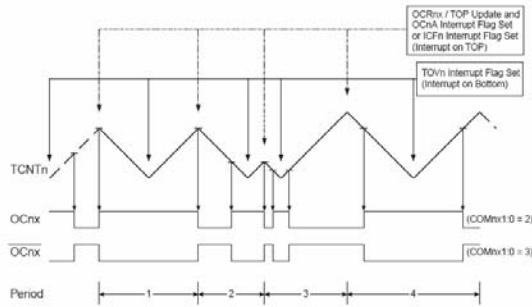


Fig.2 An example of the operation of the Atmel ATmega8 timer peripheral in a PWM mode.

2.1 Disadvantages of traditional approach

This approach to PWM generation is both easily implemented and understood and is almost universally adopted. It does however have some limitations of performance.

2.1.1 PWM period – resolution trade off

A fixed relationship between the PWM period and the PWM resolution exists for a given counter clock frequency. Assuming a sawtooth carrier,

$$\text{PWM resolution (counts)} = \frac{\text{PWM period}}{\text{clock period}}$$

$$\text{PWM resolution (bits)} = \log_2 \left(\frac{\text{PWM period}}{\text{clock period}} \right)$$

Three example processors are tabulated to demonstrate the trade off of power consumption against clock frequency. For a given clock frequency, PWM frequency or resolution must then be traded off. Low power, high PWM frequency and high PWM resolution cannot be achieved simultaneously.

Micro family	I _{CC} (3.3V), Clock freq	PWM freq at 8 bit res	PWM res at 100kHz
TI MSP430 [2]	0.5 mA at 1 MHz	3.9 kHz	10 counts 3.3 bits
Atmel AVR [1]	6 mA at 8 MHz	31 kHz	80 counts 6.3 bits
TI LF240x DSP [3]	80 mA at 40 MHz	156 kHz	400 counts 8.6 bits

One approach to overcoming this resolution limitation called Resolution Corrected Modulation is suggested by Handley and Boys [4]. By correctly alternating between adjacent duty cycle values on successive PWM cycles, a higher resolution is achieved when averaged over a number of cycles.

The software to achieve this is reasonably simple, but still creates a very high software overhead for a high PWM frequency since these calculations must be performed for every PWM cycle.

2.1.2 Quantised PWM frequency selection

A low PWM period count also leads to a very coarse selection of possible PWM frequencies, that is, an inability to accurately target a desired PWM frequency.

$$\begin{aligned} \text{PWM frequency quantisation (Hz)} &\cong \frac{\text{clock period}}{(\text{PWM period})^2} \\ &= \frac{(\text{PWM freq})^2}{\text{clock freq}} \end{aligned}$$

Clock frequency	Separation of possible PWM frequencies at 100kHz
1 MHz	10 kHz (91, 100, 111 kHz)
8 MHz	1.25 kHz (98.76, 100, 101.26 kHz)
40 MHz	250 Hz (99.75, 100, 100.25 kHz)

3. PWM GENERATION USING ADDERS

An alternative method of digitally generating a PWM waveform is found buried in most Direct Digital Synthesis (DDS) hardware implementations [5]. Each clock cycle, a phase accumulator register is incremented by a user defined value until the register overflows and wraps back around zero. In DDS, this sawtooth waveform represents the phase angle of a sine wave and is indeed subsequently converted to a sine wave usually via a lookup table.

For PWM generation, we use the sawtooth waveform directly, comparing it to a duty value to create a PWM waveform. The complete block diagram of the digital circuit shown in fig.3 is no more complex than that using a counter.

Note that in this approach, the PWM period is changed by changing the *slope* of the sawtooth waveform, and the amplitude of the sawtooth remains constant at the maximum count of the phase accumulator. This is in contrast to the counter approach which has a fixed slope and changes the period by changing the maximum amplitude.

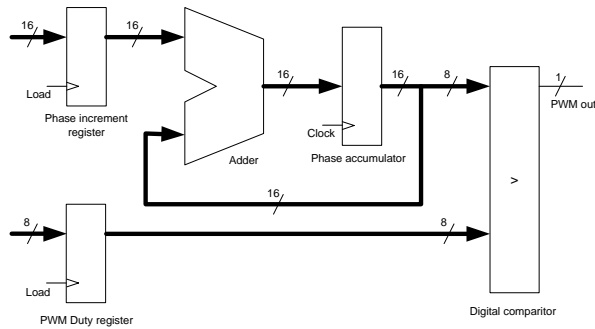


Fig.3 A block diagram of the DDS derived phase accumulator approach to generating a sawtooth and subsequently a PWM output waveform. This example implementation has a 16 bit phase accumulator and an 8 bit PWM duty register and comparator.

3.1 Advantages of phase accumulator approach

This constant amplitude, variable slope carrier leads to several advantages:

- The full amplitude of the digital comparator is always used, leading to a fixed PWM resolution equal to the full number of bits of the comparator. At high frequencies, this resolution may only be apparent when averaged over a number of cycles.
- Because of the fixed sawtooth amplitude regardless of frequency, the gain of the PWM block is constant which eases the design of control loops including the PWM transfer function.
- A fixed amplitude sawtooth makes implementing multiple phase shifted carriers for multilevel converter modulation relatively easy. A fixed offset is added (but not accumulated) to the base accumulator value to generate a fixed phase shift of the second and then subsequent carriers. This may even be done with the same adder hardware with appropriate state machine logic.
- Further, because of the constant gain, the PWM frequency can be easily changed cycle by cycle without disturbing the control loop simply changing the value of the phase increment. This allows the easy implementation of frequency spreading techniques, or converters which require PFM as well as PWM.
- The PWM carrier waveform can be phase locked to another external or internal signal by

appropriate small changes to the phase increment value.

- Note that the carrier with the appropriate choice of phase increment value already alternates between two adjacent PWM period counts to achieve the exact frequency when averaged over a number of cycles. This in itself leads to some spectrum spreading.

3.2 Hardware design

A large number of phase accumulator bits allows the generation of very low frequencies. More importantly, it guarantees any frequency can be accurately chosen and reproduced. For DDS, 24 to 48 bit phase accumulators are common. For PWM a 16 bit accumulator would be acceptable.

The frequency of the sawtooth waveform represented by the phase accumulator value is determined by how frequently that accumulator overflows. Note however that the period of the PWM frequency generated will have a jitter equal to the period of the clock frequency. As such, it is only the average period (frequency) over many cycles which can be accurately set.

$$\text{PWM frequency (Hz)} = \frac{\text{phase increment} \times \text{clock freq}}{2^{\text{accumulator bit length}}}$$

$$\text{Phase increment (counts)} = \frac{\text{PWM freq} \times 2^{\text{accum. bit length}}}{\text{clock frequency}}$$

Clock frequency	Lowest possible frequency and frequency resolution for given phase accumulator length		
	8 bit	16 bit	32 bit
1 MHz	3.9 kHz	15 Hz	0.00023 Hz
8 MHz	31 kHz	122 Hz	0.0019 Hz
40 MHz	156 kHz	610 Hz	0.0093 Hz

The number of PWM duty register bits can be chosen independently of the number of phase accumulator bits. Since the accumulator always counts from zero until it overflows and wraps around, the PWM duty register will produce the correct result if compared with the most significant bits of the phase accumulator. Because the phase accumulator may increment in steps much larger than a single count, a greater than comparison must be used rather than an equality comparison.

3.3 Numerical Example

To explain the technique better, the example of generating a 22kHz PWM waveform with a 1MHz clock is considered. In a conventional timer based approach, the required period of 45 μ s (giving 22.22kHz) is generated by counting from 0 to 45 at a 1MHz rate, then resetting to zero again. The maximum count of 45 allows only a PWM amplitude resolution of slightly better than 5 bits, and the frequency accuracy is also limited.

If an 8 bit adder is used instead of a counter, the appropriate fixed increment of 6 added at a 1MHz rate will overflow the adder after 45 μ s. The straight line thus created has a constant amplitude rather than constant slope and so has a fixed gain. The default behaviour of the adder implements modulo arithmetic such that the overflow is not back to zero but to a different remainder each cycle. For this example the count sequence will be 0, 6, 12, 18, ..., 246, 252, 2, 8, 14, ..., 248, 254, 4, 10, ..., 250, 0, 6 etc. This cycle produces two 43 μ s periods followed by one 42 μ s period for an average frequency of 23.4kHz. This has the beneficial effect of blurring the PWM frequency spectra slightly. The amplitude of the carrier is between 0 and 255 so a full 8 bit resolution is available upon comparison.

Phase shifted carriers for multilevel modulation are easily generated by adding a phase offset to the first carrier. To generate four equally spaced phase shifted carriers, offsets of 64, 128 and 192 are added (but not accumulated) to the accumulator value before comparison (see fig.4).

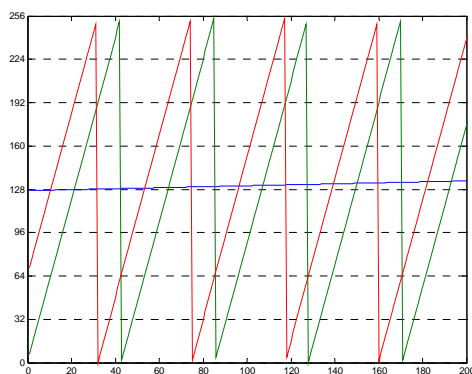


Fig.4 The first 200 μ s (200 clock cycles) of the 22kHz PWM example. Shown are the 8 bit phase accumulator output (green), a second carrier generated by adding a fixed offset to the first carrier (red), and the very beginning of a 50 Hz sin wave (blue) from which the PWM waveform is generated.

It may be noted that to generate the maximum length sequence of values in the phase accumulator register and to ensure the full resolution is achieved, an odd phase increment should preferably be chosen. This ensures every possible phase value is visited once before the sequence repeats and limit cycles will be avoided. In the example presented, an even phase increment of 6 led to only even phase values being chosen and the sequence repeating after 128 increments rather than 256.

A 16 bit adder and accumulator register would be a more realistic hardware implementation. An odd phase increment of 1441 achieves a PWM frequency of 21 988 Hz from a 1 MHz clock, with a sequence that only repeats after every 65536 counts or 15 Hz.

4. SPECTRAL PERFORMANCE

The spectral performance of this technique of PWM generation is excellent as seen in fig.5. Harmonic lines of the carrier are somewhat smeared in frequency, reducing their peak amplitude. However the fundamental synthesized waveform is reproduced accurately without distortion. The case shown is for the example case presented, with a 8 bit phase accumulator and an 8 bit PWM comparator. The phase increment of 6 produces a PWM carrier frequency of 23 kHz from the 1 MHz clock. A 50Hz fundamental sine of 90% modulation depth is reproduced faithfully.

5. CONCLUSION

The PWM generation technique presented using a phase accumulator is no more complex to implement than the currently favoured counter approach. It has numerous advantages including a fixed gain, full resolution regardless of PWM and module clock frequencies, accurate frequency generation, and the ability to modulate and phase lock the carrier frequencies. Additionally the generation of multiple phase shifted carriers suitable for multilevel modulation is a trivial extension. The spectral performance is better than conventional PWM as the fundamental has high accuracy while the carriers have lower peak energy. Future work will focus on experimental results for multilevel work, and the demonstration of some of the more advanced capabilities such as phase locking.

6. REFERENCES

[1] Atmel Corp, Atmel ATmega8 datasheet, rev.2486M-AVR-12/03, doc2486.pdf, available from <http://www.atmel.com/>

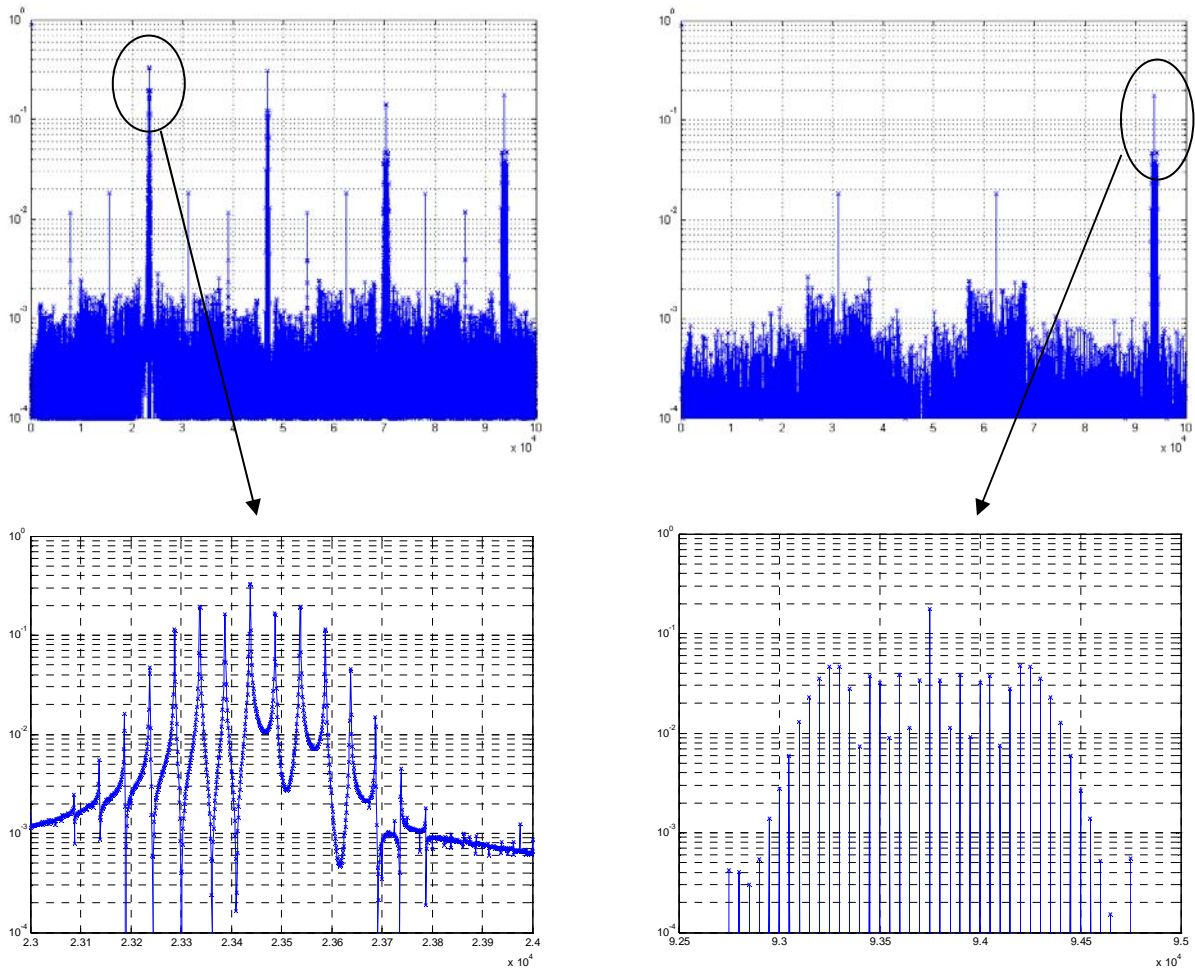


Fig.5 The PWM spectra for a 50Hz fundamental with modulation depth of 0.9 generated by a 22kHz PWM waveform. The right hand plots show the cancellation achieved in a five level multilevel converter with four carriers with equal $\pi/2$ phase shift between them. The 50Hz fundamental (on LHS axis of top plots) is completely undistorted with all surrounding harmonics below $10e-4$.

[2] Texas Instruments, MSP430x13x, MSP430x14x Mixed signal microcontroller datasheet, SLAS272D - JULY 2000 - REVISED MARCH 2003, available from <http://www.ti.com/>

[3] Texas Instruments, TMS320LF2406A DSP controller datasheet, SPRS145I - JULY 2000 - REVISED SEPTEMBER 2003, available from <http://www.ti.com/>

[4] P. G. Handley and J. T. Boys. "Resolution corrected modulation: the practical realisation of ideal PWM waveforms". IEE Proc-B, 139(4):402-408, July 1992.

[5] Analog Devices, Inc, "A Technical Tutorial on Digital Signal Synthesis", 1999,

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