

**PV Module  
Series String Balancing Converters**

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**6<sup>th</sup> November 2002**

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# Abstract

Developments in global policies have seen the push for greater use of renewable energy sources. This has led to increased usage of medium sized PV arrays in homes and businesses. The panels are usually joined in series to get higher voltages better matched to the grid. However, when modules are joined in series they will experience mismatched power outputs that can lead to significant losses in the array. This mismatch comes from shading, differing orientation of modules and different panel characteristics in the array. There are several methods to combat this already being developed or marketed. However, these are either inefficient or require each system to be matched to the PV array as the systems are centrally controlled.

This thesis attempts to address these problems by making module converters that can be placed in each junction box of a PV module. This eliminates mismatch between modules by Maximum Power Point (MPP) tracking each module. If a module is generating less current than the rest of the array, the converter balances the output of the module allowing it to still operate at its MPP. A photovoltaic array of 12 panels, each able to generate 15V 3A is designed for. Cuk converters are used to connect each PV module with the preceding module. A Flyback converter is used to connect the first panel in the array to the last panel. This configuration allows for power to be shifted from any PV module to a module that needs to be balanced. In the current prototype the Cuk has a peak efficiency of 88% and the Flyback an efficiency of 84%.

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Dear Sir,

In accordance with the requirements of the Degree of Bachelor of Electrical Engineering (Honours). I present the following thesis entitled “**PV Module Series String Balancing Converters.**” This work was performed under the supervision of Dr Geoffrey Walker.

I declare that the work submitted in this thesis is my own work, except as acknowledged in the text, and has not previously been submitted for a degree at the University of Queensland or any other institution.

Yours sincerely,

John Xue

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## **2.0 Acknowledgements**

Dr. Geoffrey Walker initiated the founding ideas behind this thesis and provided insight and valuable information into many of the problems that were encountered. His positive attitude throughout the duration of this thesis always put things into perspective whenever difficulties arose. This thesis would not have been possible without him.

There are many other people that have contributed directly or indirectly to this thesis. Some acting as sounding boards, sources of information, or providing resources that contributed to the development of my electronics. While their individual contributions have been small, their efforts have still been greatly appreciated.

Finally, I would like to thank my family and friends for keeping me sane.

## 3.0 Introduction

*Development of balancing MPPT converters linked in parallel to a series string of photovoltaic modules.*

Recent developments in global policies have seen the push for more environmentally friendly energy sources, with the Kyoto Protocol [1], a prominent example. As a result there has been renewed interest in developing renewable energy sources such as wind, hydro, and solar.

Last century, solar panels were mainly being used in small-scale devices independent or remote from the grid, or for large-scale power generation. In the last few years, with government subsidies in countries such as Japan, Germany, Switzerland and the USA (See references [2], [3], [4], [5]), Solar energy has been increasing used in medium sized grid connected PV (photovoltaic) systems. These are now being purchased by households or by private companies to supply power to buildings.

Most of these PV systems are arranged in a series string of PV modules to generate a usable amount of voltage, as otherwise they would generate very low voltages. Generally PV arrays have a converter that handles the entire string, and do not maximum power point track (MPPT) for individual modules in the array.

This thesis will attempt to place converters over each module in the array, and so allow each module to operate at its maximum power point. This should dramatically reduce problems such as mismatch between panels and different power output due to differences in panel orientation, shading problems, and modularity problems.

Previously it has been accepted that such a configuration would involve significant losses in the converters, as all the power would be shifted through each converter on the series string. However, power loss can be significantly decreased if only the mismatched amount of power is shifted around each module.

It is hoped that this converter configuration would be both efficient and cost effective enough to be included by default on each PV module sold. The additional cost should be offset by the increased power output potential of the modules in a series string. The design will also take into account installation time, so the set up of the array will be minimal with no adjustment to the modules to cater for different array sizes.

This thesis will give background information about the maximum power point problem, and current solutions in development or on the market. Explanations into the design of the system and details of the implementation were explained as clearly as possible. The thesis concludes with an analysis of the hardware evaluating what was achieved.

While explanations of much of the theory is covered, good knowledge of power electronics is recommended, as this thesis does not have time to cover basic issues.

## 4.0 Literature Review

### 4.1 The Problems to be Overcome

PV modules are set of photovoltaic cells in series, and have a maximum power point (MPP). The MPP is the voltage point where a photovoltaic cell, module or array will generate the maximum electrical energy for a given illumination level. In practice the MPP is not always obtained.

Most PV arrays are arranged in a series string, the modules connected in series one after another. This is done to generate higher voltages better matched to grid connection. This means that according to Kirchhoff's current law, the modules will all experience the same current running through them. If the modules are all generating the same amount of power then this poses no problem. However, when modules are generating different amounts of power then some modules will be operating away from their MPP. This can be due to panel mismatch, where panels in an array are generating different amounts of energy due to manufacturing tolerances or temperature differences. Another cause is due to orientation mismatch, where panels are placed on a roof at different angles to the sun so they generate different amounts of power. Finally even shadows reducing the sunlight being received by a single panel can reduce the power produced by the entire array.

The energy lost when mismatched power output occurs is surprisingly large. When a module is partially shaded not only does it cause other modules to deviate from their maximum power point, but it can also become reverse biased. When this happens the shaded module begins acting as a load, dissipating the energy generated by all the other modules in the string. Lindgren [6] performed some shading experiments with cells. In the worst-case scenario, for one cell totally shaded in a 24 series string, the energy reaching the cells was reduced by 4.16%. However, the power output was reduced by 48.2%. Cell and module shading exhibit similar behaviour, and it can be expected that an experiment with module shading would yield similar results.

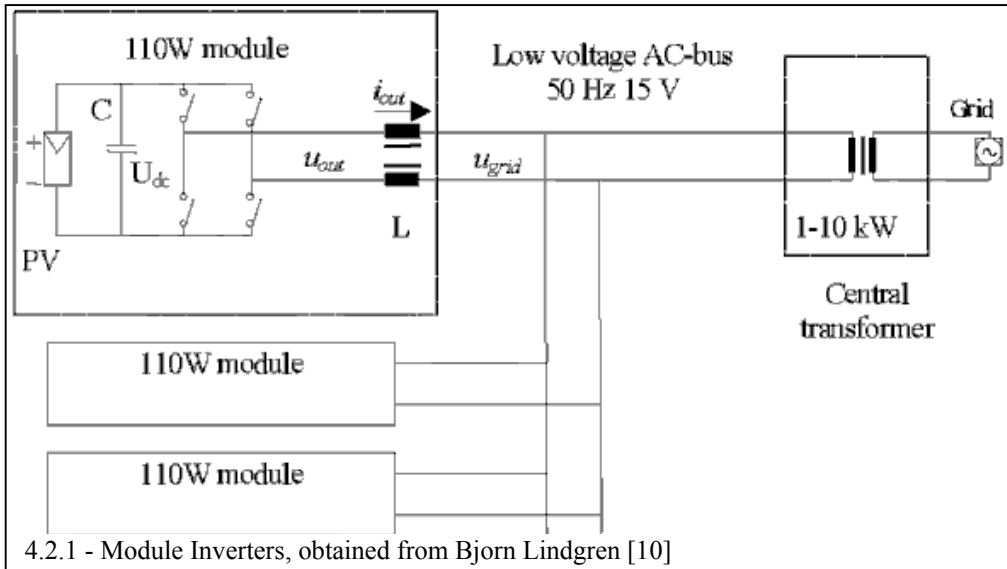
## **4.2 Methods Currently Being Used**

The main solution for the panel mismatch problem has been grading and grouping of panels with similar characteristics at the factory and research into better manufacturing techniques.

Bypass diodes are a low cost method to reduce the effects of local shading. A diode is placed as an alternative shunt path for current around shaded cells in series strings. Usually one diode is placed in parallel with every 18 cells (half a 12V PV module).

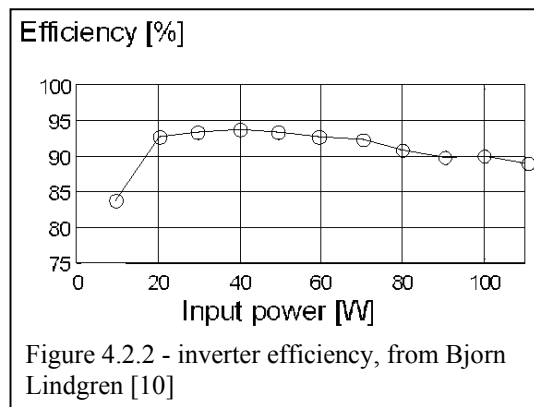
The shading problem has been approached in a number of ways. The commercially available options are parallel module inverters. Examples are No Outage's 120VAC solar module [7], and the SunSine 300 by Ascension Technology [8]. Plug and Power by Pacific Solar [9] is an Australia product that uses a module inverter generating directly to 240V. AC solutions give a modular design, if one module fails or experiences shading none of the other modules are affected. It also allows for extremely easy installation that any electrician will be able to perform.

There are a few disadvantages of this approach, which stem from complexity of these converters. Every PV module converter generally requires at least two successive power conversion stages, one of them usually including isolation. This lowers efficiency and increases costs. The problem is made more difficult by the high reliability required in the harsh environment that PV modules operate in.



Bjorn Lindgren [10] gives the design of a parallel AC bus system shown in Figure 4.2.1. In addition to being modular, this design contains few components therefore increasing its reliability. On the down side, due to the low voltage of the bus, high currents have to be handled by the bus and control circuitry increasing losses. Furthermore, 25V DC is required from each module and at low irradiation the circuit will be unable to function. Lastly, the output frequency of 50Hz to match the grid, requires that the circuit have large input capacitors to prevent a 100Hz ripple from affecting solar modules.

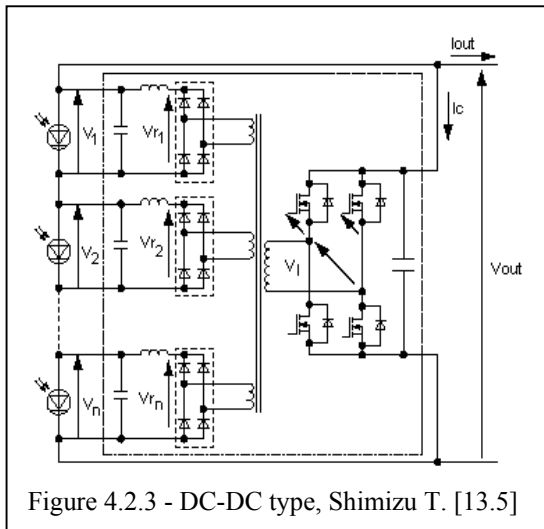
All of the power from the PV modules is channelled directly through the converter, and consequently a percentage of all power output is lost. The AC solution by Lindgren loses 7 to 10% of the power output from the converters. This is shown in the efficiency graph of his inverters, Figure 4.2.2.



While significant effort has been invested in AC modules, often the shading losses do not justify the general loss in efficiency and the cost of the electronics. Quoting from Konrad Mauch Chief Technology Officer at Xantrex Technology Inc. [11], “AC modules that integrate a small inverter directly with the PV module have not been commercially successful, despite considerable development effort”.

There is also research occurring in Switzerland that is developing an inverter that can be placed over individual PV cells [12]. While this does mean that mismatches will be eliminated, the inverters have to be specially constructed to minimize all losses. Practical efficiencies will be extremely hard to achieve, especially since the inverters are being designed for 1-2V and 100A.

The most promising topologies to address the shading problem has been explained in Generation Control Circuit for Photovoltaic Modules by Toshihisa Shimizu and his research group [13]. They have two topologies that they discuss, a DC-DC converter type and a multi-stage chopper.



The DC-DC converter type is simple topology (Figure 4.2.3) that has converters over each module and sets the same voltage for every module. Power is transferred from the output of the array to each module via a transformer. This method allows for different modules to generate different currents and hence different power outputs, but doesn't allow for individual tuning of each module's voltage.

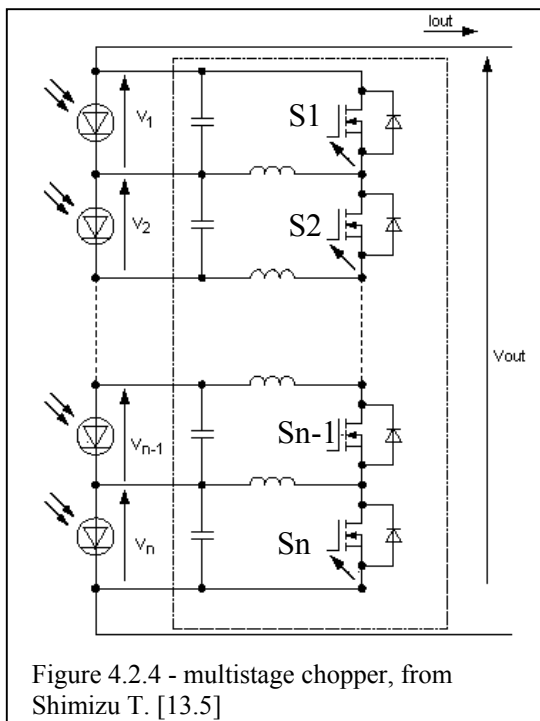


Figure 4.2.4 - multistage chopper, from Shimizu T. [13.5]

The multistage chopper is a series of bi-directional converters over each PV module (Figure 4.2.4). These are centrally controlled, but unlike the DC-DC converter type the multistage chopper allows for each converter to be individually controlled. Figure 4.2.5 showed the gate source voltage of the switches. The off time of the switch is when current flows through the PV module and hence energy is drawn from the module. The percentage of power drawn from each module is proportional to the switch off duty cycle, so precise control over each individual module is achieved.

The main problem with the multistage chopper and the DC-DC converter is the lack of modularity. Both are centrally controlled and modules cannot be removed or added without adjustments in the designs.

To summarize, previously there have been several approaches to the problems of PV module mismatch and module shading. Grading and grouping had been the best solution so far to PV module mismatch. However, testing and grouping PV modules costs money and cheap hardware that eliminates this, could possibly save money. There has been extensive research into inverters that eliminate losses due to shading. These DC to AC inverters often do not have efficiency high enough to justify their cost and their internal losses. Another solution to the shading problem is the Generation Control Circuit, it

allows for precise control over each module eliminating shading losses, but it is centrally controlled and cannot be resized easily for varying array sizes.

### 4.3 Maximum Power Point Tracking

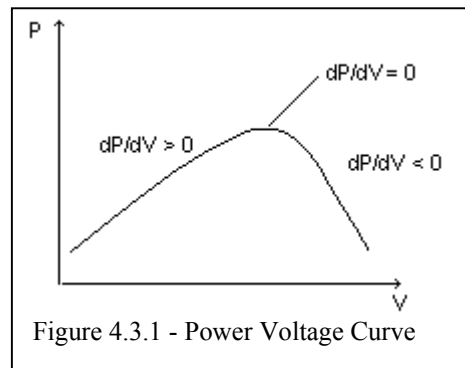
Maximum power point tracking (MPPT) allows the photovoltaic module to operate at its maximum power point. It is done using a converter that regulates the power that is drawn from the converter. By varying the duty cycle of the switches, the energy transferred through the converter can be precisely controlled.

The maximum power point (MPP) is usually monitored through two control variables. Either voltage or power is measured to determine whether the solar array is at maximum power point [14]. This is used in a feedback loop back to the converter to determine the maximum power point.

When the system uses voltage, it regulates the solar array to a specific voltage that should give the maximum power point. The MPP voltage is usually varied based on a fixed ratio of the open circuit voltage [15]. This mostly removes the dependence on temperature and irradiance.

There is a similar method that tracks the MPP by setting the module current to a fixed ratio of the short circuit current [16].

When power is used as the control variable, the maximum power point is obtained by changing the derivative  $\Delta P/\Delta V$  to zero. This is the condition for the top of the crest in power output as seen in Figure 4.3.1. This does mean that the characteristics of the solar array do not have to be known. This maximizes the power transferred to the load not the power obtained from the solar array.



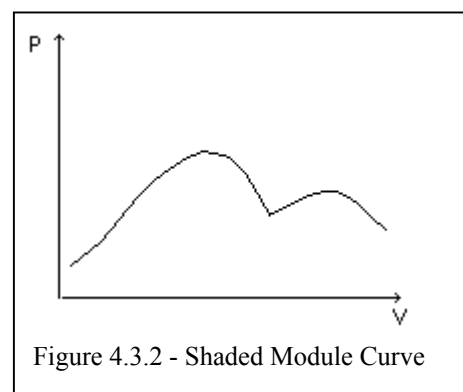
There are many ways of tracking the maximum power point [14]. Three of the common tracking algorithms are; curve fitting, Perturb and Observe, and Incremental Inductance.

The curve fitting technique stores the solar panel's characteristics into a mathematical function and maps a panel's power point from the formula. This method avoids heavy runtime calculations, but fails to consider such things as temperature changes and shading [17].

In the Perturb and Observe method, the operating voltage is periodically increased or decreased. Then power output is observed, and the operating point is adjusted accordingly. This is a method that is often used, as it requires only the voltage and current, and is simple to implement [14]. This is termed a hill climbing technique, as the algorithm slowly climbs up the power curve to the maximum power point.

The Incremental Conductance method can also measure where the MPP is relative to the current operating voltage, and gives better results than the Perturb and Observe method. Instead of measuring the power output it calculates the conductance and the incremental conductance. When the conductance is larger than the incremental conductance, the operating voltage is lower than the MPP. When the conductance is smaller, then the operating voltage is higher than the MPP. The maximum power point is where the conductance equals the incremental conductance [18]. This method uses four sensors to measure MPPT.

Figure 4.3.1 describes a PV array that is acting normally. When partial shading of an array occurs, as seen in Figure 4.3.2, the above methods may obtain the wrong power peak as they incrementally seek the MPP. This can be avoided by doing additional things, such as sweeping the full voltage range every minute or so.



## 5.0 Scope of the Thesis

### 5.1 Initial specifications

The design was specifically targeted for the 12 solar panels on the roof of the Axon building at the University of Queensland. The five that retained their labels have the following characteristics.

Table 5.1.1 – Solar Panel Characteristics

	STC	STC	STC	STC	STC		at T	at T	calc'ed	
mod	Pmax	Voc	Isc	Vpmax	Ipmax	T	Pmax	Ipmax	Vpmax	Serial no
1	59.3	20.6	3.91	16.4	3.61	49	42.6	2.9	14.69	A99C 2347791
2	61.6	20.8	4.01	16.4	3.75	49	44.4	3	14.8	A99C 1347718
3	60.4	20.7	3.96	16.3	3.7	49	43.4	3	14.47	A99C 1347680
4	60.1	20.8	3.92	16.3	3.68	49	43.3	2.9	14.93	A99C 1347686
5	60.9	21.5	3.99	16.8	3.62	47	44.4	2.89	15.36	A0004 27404815

Under normal environmental conditions, each photovoltaic module generated about 3 Amps at 15 Volts. However, the circuitry must be able to withstand fault conditions of 20V, 4 Amps. The assumption was made in many of the calculations that the input and output would be 15V, as the maximum power point will generally be found near that voltage.

The junction box of the PV modules allowed for PCB mounting of size 67mm by 107mm with a clearance of 22mm above the PCB.

Starting with these specifications and the new concept of only shifting the minimal amount of power to Maximum Power Point Track, a design must be created.

### 5.2 Objective

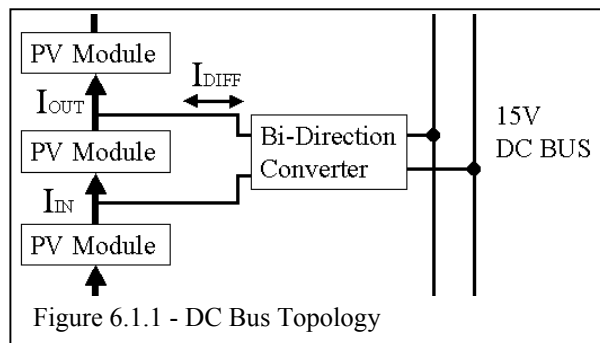
The final objective of this thesis was to create maximum power point trackers that shift power between modules to equalize the PV modules in a solar array. This required construction of converters and writing the software to perform the maximum power point tracking.

# 6.0 Design

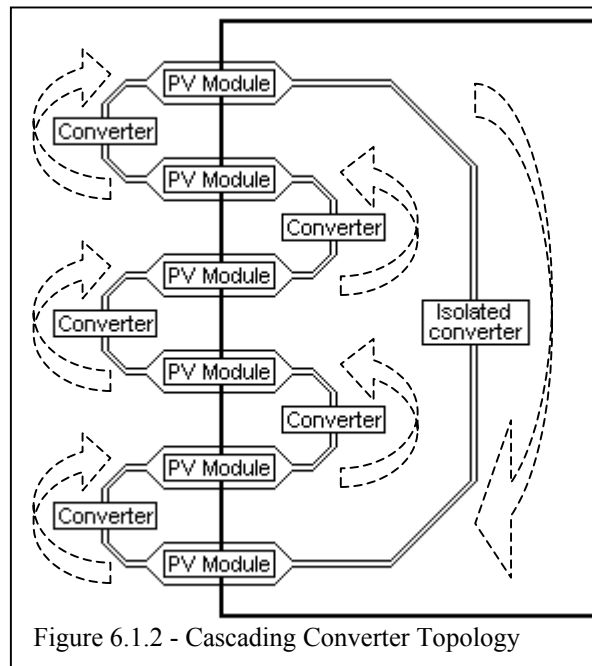
## 6.1 Overall Topology

As explained earlier, series string PV arrays suffer from power loss, because the same current must flow through every one of the PV modules. Modules differ in their characteristics and also in the amount of illumination they receive. This mismatch prevents PV modules from operating at their maximum power point. To allow each panel to operate at their maximum power point, converters could be placed to reroute current so that all the modules can operate at peak efficiency. Two different implementations are discussed.

The first topology, seen in figure 6.1.1, involves uses a bi-directional converter that reroutes current through a DC bus. This must be an isolated topology as there is no common ground between the modules. While the overall design is simpler, the complexity and cost of the converters is greater as all the converters need to be isolated.



The other topology is a cascading converter topology and can be seen in figure 6.1.2. It draws power from previous PV modules through the string of converters that run in parallel to the PV modules. Excess current is routed through the converters eliminating panel mismatch. For this topology to work an isolated converter is required to close the power loop, and supply the first module of the series string.



For the cascading converter topology, a non-isolated converter is also suitable to close the power loop. It drains power from the combined output of the solar array and steps the voltage down before feeding it back into the first PV module. However, losses are usually experienced with a large step down in voltage, while unity gain in a converter generally gives the best efficiency. Furthermore, this kind of converter works best for fixed array sizes.

The Cascading Converter Topology is used in this thesis. The converters are simpler and require fewer components than the DC Bus solution. This means that the converters would be cheaper to construct and hence this topology gives better value for money. However, this topology might be unstable requiring highly intelligent software to run it efficiently. An efficiency and cost comparison of both solutions should be completed in future work.

There are two main sections of the hardware, the isolated converter and the cascade converter. While the requirements of these two sections are different, the differences are purposefully limited to the converter design. This saves considerable redesign work of the non-converter electronics. With the first leap from theory to design, a block diagram of the actual hardware is generated.

Figure 6.1.3 is derived from the way a MPPT device works (Section 4.3). Various characteristics are sensed, these characteristics are fed into the maximum power point tracker, and the converter is switched adjusted so that the converter places the PV module closer to the maximum power point.

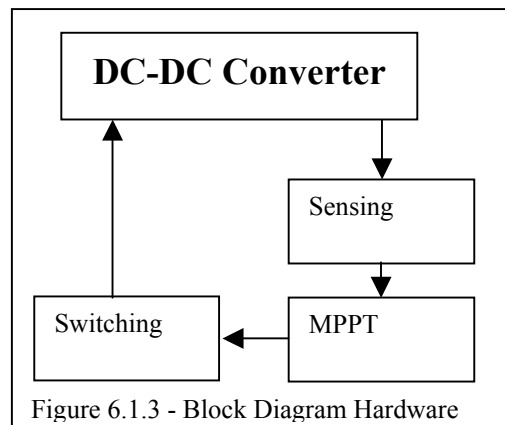


Figure 6.1.3 - Block Diagram Hardware

Next decisions are made on what kind of algorithm should be used to perform the MPPT. This determines what kind of sensing circuitry is required. The Perturb and Observe method, mentioned in section 4.3, is the simplest method of maximum power point

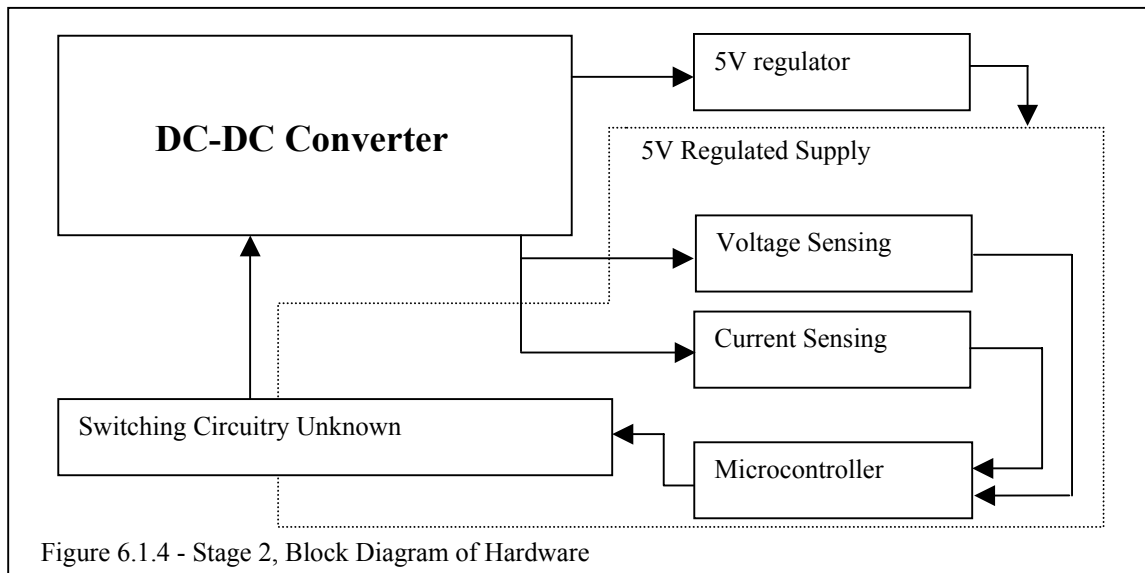
tracking. Research indicates that it requires a current sensor and a voltage sensor on the module that needs to be tracked. The theory for this algorithm is used as the basis for a new algorithm that will be explained in section 6.7.

The MPPT is performed by a microcontroller. This is the easiest method to develop a suitable tracking algorithm, and made changes to the tracking much easier to implement. The sensors generate analogue values, so an analogue to digital converter is required. Many microcontrollers have these internally, so this does not generate extra hardware.

The microcontroller and the sensing require a regulated source. Since microcontrollers mostly operate at 5V, a 5V regulator is required to supply this circuitry.

The remaining design of the switching cannot easily be designed using a top down approach. How the converters are switching is heavily reliant on the topology of the converter and the requirements of the converters.

Figure 6.1.4 shows what had been designed using the top down approach.



Substantial theory is required to complete the design. The following sections briefly cover the various design issues and generate a bottom up approach to complete the switching circuitry. Various other design issues integral to the design are also addressed with minimal detail.

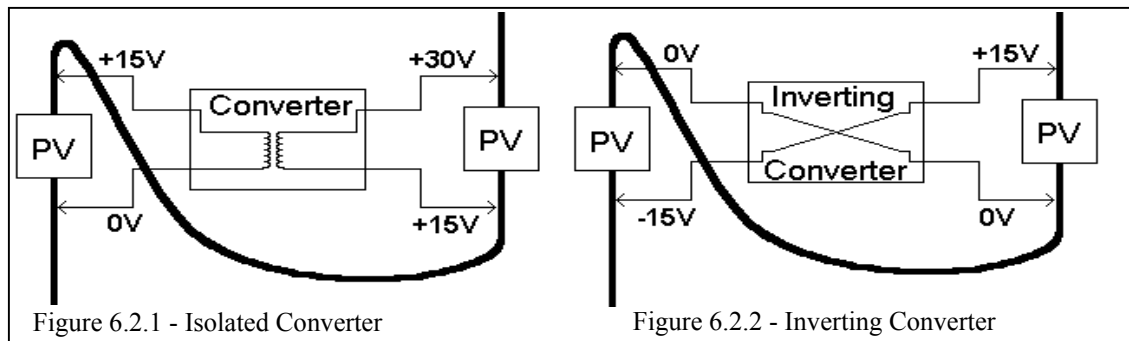
## 6.2 Converter Characteristics

The requirements of the converter are extrapolated from section 5.1 – “Initial Design Specifications”, and the theory of the topology in section 6.1.

For power characteristics, the converters are designed to take maximum load of 3A, with reasonable efficiency at very much lower currents. The circuitry should be able to tolerate a maximum of 4A in fault conditions. The voltage is centred at 15V for both input and output of the converters with voltage swings expected up to 20V and down to 7V.

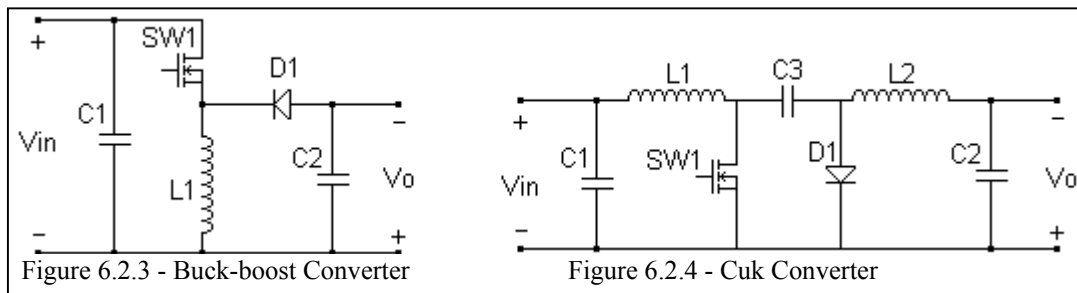
Careful analysis of the Cascading Converter Topology discussed in section 6.1 reveals that there are two main topology attributes that are required of the DC-DC converters.

Firstly, the converter needs to shift power to an output voltage that can be either higher or lower than the input voltage. This is required because the maximum power point of a PV module may be either lower or higher than the voltage of the previous module that powers the converter. Secondly, the converter must be inverting. This allows for the input and output of the converter to share a common reference point, and hence it will not require isolation.



In Figure 6.2.1 the converter does not invert and without isolation the 0V of the first PV module connects directly to the +15V of the 2<sup>nd</sup> PV module. This results in a short circuit. In Figure 6.2.2 the converter inverts and the point between the two PV modules can be treated as the reference point that the converter switches around. Isolation of the converter is not required in this case.

There are two common converters that fulfil these requirements, the Buck-Boost and the Cuk converter. These are shown in Figures 6.2.3 and 6.2.4.



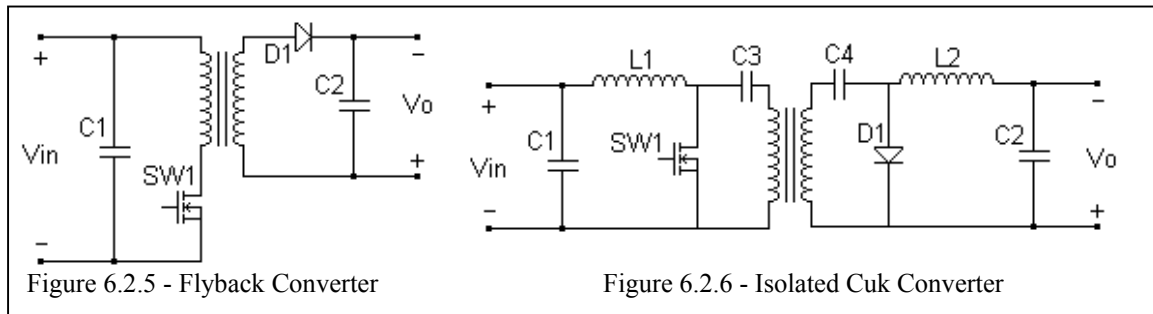
While these two converters are able to perform the same function, DC-DC inverting step up or step down conversion, they operate in different ways. The buck-boost converter stores energy into its inductor over the switch on cycle and releases that energy in the off cycle. The Cuk converter stores all of its energy in the capacitor. The important points to consider with choosing between the two topologies are cost, efficiency and how the converter may affect other circuitry.

The Cuk converter requires more components than the buck-boost and consequently costs more to construct. Its redeeming feature is that unlike the buck-boost there is very little ripple observed on both input and output, so the impact on the rest of the circuitry is small. The efficiency of the Cuk and the buck-boost are comparable and would require significant testing to determine, which would be most efficient for the application.

The main priority of this thesis will be exploring the concept of MPPT converters linked in parallel to a series string of PV modules. Consequently, the main considerations in choosing the converter topology will be creating a working prototype. This means that how the converter affects the rest of the design is the most important issue as this impacts on the success of the prototype. Hence, the Cuk converter was chosen for the DC-DC converters.

The Cascading Converter topology requires an isolated converter to close the power loop. This allows the first few converters to MPPT effectively as those later in the series string.

Two kinds of converters are considered, the flyback converter [19], which is an isolated variant of the buck-boost, and an isolated Cuk converter [20]. These are shown below.



These isolated converters work in a similar way to their non-isolated counterparts. In the Flyback (Figure 6.2.5) the transformer replaces the inductor of the Buck-Boost and energy was stored in the transformer. In the Isolated Cuk the centre capacitor still stores the energy, only with the capacitor split in half by a transformer. With the isolated Cuk the centre capacitors need to be larger than its non-isolated counterpart, as  $C3$  and  $C4$  in Figure 6.2.6 shows that the two capacitors are in series thus have a reduced combined capacitance.

Both the Cuk and the buck-boost were simulated in Pspice. However, it was decided that an isolated Cuk converter would be more difficult to implement from both simulation results and research. Hence, the flyback was chosen as the converter to be used to close the power loop.

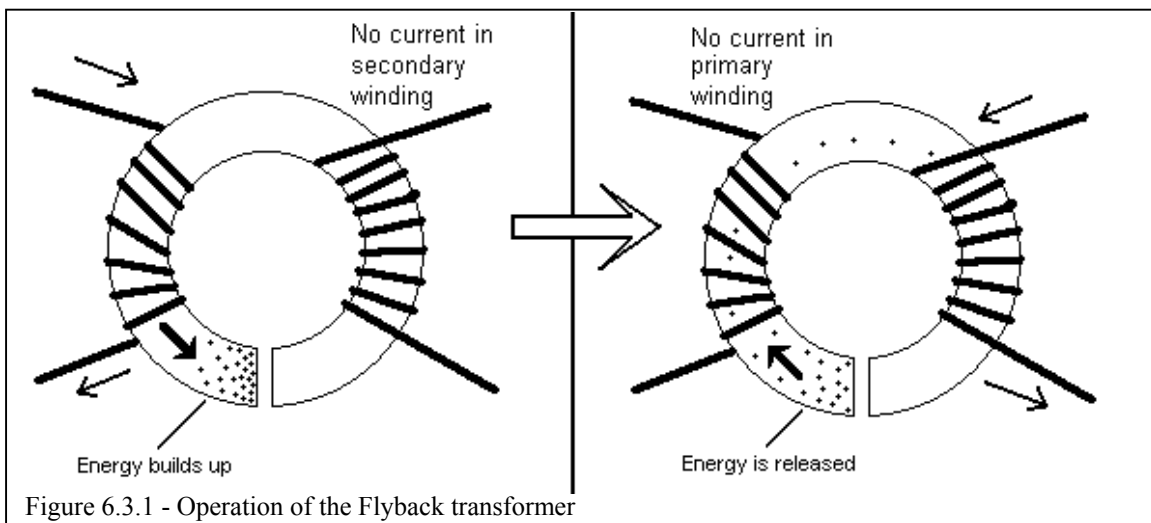
### 6.3 Flyback Transformer Design

Designing a transformer can be an extremely confusing process, especially since all the books that detail transformer design require a table of Maximum V-I ratings of cores to be available and these were not available. So this section on transformer design gives a step-by-step guide on transformer sizing, air gapping, turns and flux density from first principles.

There are several kinds of transformer topology available. E-Planar are PCB transformers, the windings are manufactured on PCB and the cores are placed directly over the PCB windings. This resulted in an extremely low profile and strong magnetic coupling. The disadvantages are the limitation in number of turns, small core sizes, and difficulty in changing the number of windings in prototyping stages. Another transformer topology is the ETD, Easy Transformer Design, the main disadvantage is the height of the transformer. The EFD, Easy Flat Design, transformers have a relatively low profile while keeping reasonable core sizes, and possible number of windings. These topologies are just some of topologies listed at Ferrxocube [21].

Transformer cores are made from several different kinds of materials, but magnetically soft materials are preferred as they had a low magnetic hysteresis. This refers to their ability to magnetize and demagnetise (Tipler p911-912 [22]). The area enclosed by the magnetic hysteresis curve (Figure 29-36 Tipler p112 [22]) indicates how much energy is converted to heat when a material magnetizes and demagnetises. Hence, a magnetically soft material works more efficiently as a transformer. Soft ferrites are most commonly used for converter transformers.

As explained in section 6.2, the Flyback converter requires a transformer to store its energy. Unlike a normal transformer that stores no energy in its windings, the Flyback stores its energy in a large and purposeful air gap. Figure 6.3.1 shows how this works.



First energy is stored in the air gap by the primary winding, with no current in the secondary winding. When the Flyback completes the storage of this energy, the primary current is turned off and the energy is released through the secondary winding [23].

For a Flyback to work the air gap must be sufficiently large to hold the energy for one cycle. To calculate this, the energy that is stored in  $1\text{m}^3$  of air is found from the permeability of air and the magnetic flux through the air gap [24].

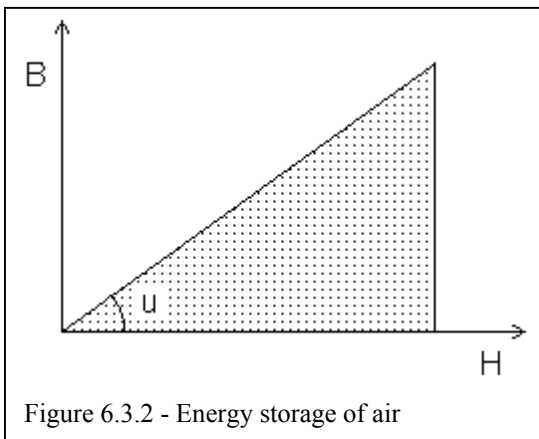


Figure 6.3.2 shows the formula  $B = \mu_0 H$  [25]. The shaded area of the graph is the energy stored per cubic meter of air,  $B$  the magnetic flux,  $\mu$  the permeability of the air, and  $H$  the Magnetic Field Intensity (Amps/meter).

Formula for energy per cubic meter of air is derived, giving  $u_m$ .

This can found in Tipler page 943 [22].

$$\text{Eq - 6.3.1} \quad u_m = \frac{B^2}{2\mu_0}$$

The energy that the air gap is required to store ( $E_{req}$ ) is found from the power that is transferred through the transformer in one cycle. Power rating divided by the switching frequency.

$$\text{Eq - 6.3.2} \quad E_{req} = \frac{P}{f}$$

From this the volume of the air required,  $V_{req}$ , is calculated.

$$\boxed{\text{Eq - 6.3.3} \quad V_{req} = \frac{E_{req}}{U_m}}$$

Then from the cross-sectional area of the transformer,  $A_e$ , and the required volume the air gap length,  $l_a$ , is calculated.

$$\boxed{\text{Eq - 6.3.4} \quad l_a = \frac{V_{req}}{A_e}}$$

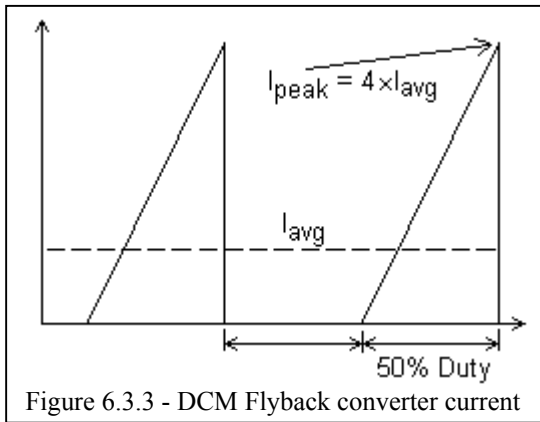
This is the minimum air gap required to store the maximum amount of energy that the converter needs to handle.

Next the maximum turns,  $N$ , is calculated such that maximum current doesn't saturate the transformer. Saturation is avoided, as when a transformer saturated it no longer transfers current to the secondary winding and the primary winding acts like a short circuit causing extremely high primary currents to be observed. This  $N$  is for the primary as the  $I_{peak}$  is for the primary.

$$\boxed{\text{Eq - 6.3.5} \quad N = \frac{\mathfrak{R} B_{sat} A_e}{I_{peak}}}$$

The reluctance of the core,  $\mathfrak{R}$ , is calculated using the reluctance of the material, plus the reluctance of the air gap.

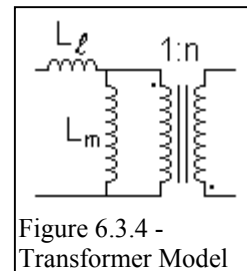
$$\boxed{\text{Eq - 6.3.6} \quad \mathfrak{R} = \frac{l_e}{\mu_r \mu_0 A_e} + \frac{l_a}{\mu_0 A_e}}$$



$I_{peak}$  is calculated using the average current and the assumption that the duty cycle is 50%. This assumption is generally true, as MPP between PV modules are always close. The current waveform of a Flyback in DCM is shown in Figure 6.3.3. Using simple geometry the  $I_{peak}$  is 4 times the average current through the converter.

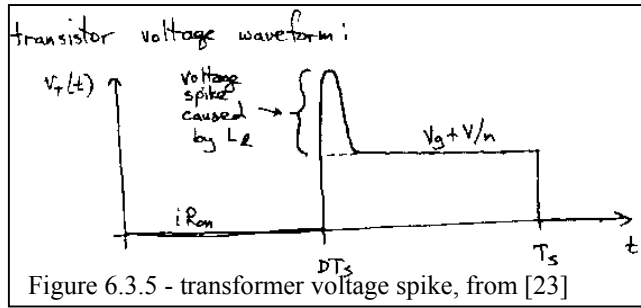
The converter is operated in DCM, as CCM in a Flyback can be unstable in its operation. CCM is avoided for the Flyback in many low power applications as the converter transfer function has a right half plane zero. The speed of feedback loop is then reduced to stabilize the control loop [26]. Section 7.1.1 gives a detailed explanation of CCM and DCM.

Figure 6.3.4 shows the transformer model. The transformer primary can be modelled as two inductances. The magnetizing inductance ( $L_m$ ) transfers the energy to the other side and the leakage inductance ( $L_l$ ), which is the inductance that doesn't magnetize the secondary.

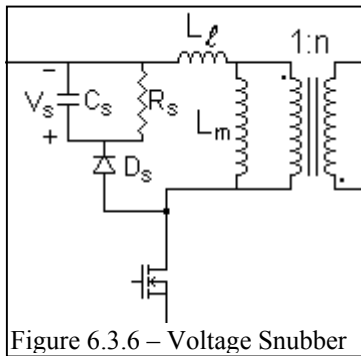


The side effect of the leakage inductance is voltage spikes over the MOSFETs when the MOSFETs are switched off. The leakage inductance of the transformer causes current to continue flowing after the MOSFET stopped conducting, resulting in the build-up of charge between the transformer and the MOSFET and generating the large voltage spike.

This is shown in Figure 6.3.5.



A voltage clamp snubber, seen in Figure 6.3.6, can be inserted to give a path for the current to flow after the MOSFET turns off. It consists of a diode a capacitor and a resistor. The full explanation on choosing  $C_s$  and  $R_s$  values is found in reference [23].



Eq - 6.3.7 from [23]

$$\frac{V_s^2}{R_s} = P_{snubber} = \frac{1}{2} L_l I^2 f_s$$

Eq - 6.3.8 from [23]

$$C_s \gg \frac{T_s}{R_s}$$

First, the acceptable amount of voltage spike,  $V_s$ , is determined.  $L_l$  the leakage inductance is either measured or estimated. The current at the time of turn off was the  $I_{peak}$  (calculated earlier). Using Equation 6.3.7 the power dissipated over the snubber is found and the necessary resistance to dissipate that power is found. Equation 6.3.8 shows the minimum  $C_s$ , chosen so the snubber does not experience significant ripple ( $T_s = 1/f_s$ ).

## 6.4 Synchronous Rectification

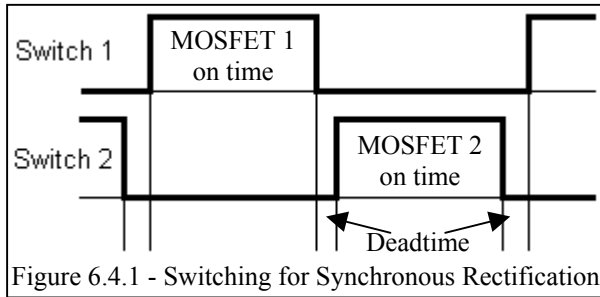
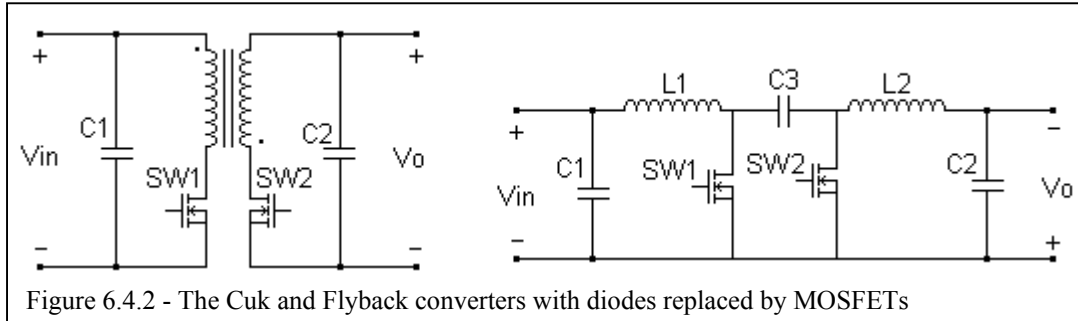


Figure 6.4.1 - Switching for Synchronous Rectification

Synchronous rectification involves using a MOSFET in the place of a diode and switching this MOSFET on in the off cycle of the other MOSFET. The gate-source voltage waveforms are shown in Figure 6.4.1.

The main advantage of synchronous rectification is the efficiency gain that results from removal of the forward drop of a rectifying schottky diode. The diode forward drop losses are magnitudes higher than the very low on resistance of a MOSFET. The diode is often one of the major sources of loss in many converters, so this results in a significant increase in efficiency. As efficiency is a major concern for the converter, synchronous rectification is included in the design.

The main danger from synchronous rectification is shoot-through, when both MOSFETs were conducting, and high currents and voltages result. This causes massive losses in the converter. Shoot-through can be avoided by inserting dead-time into the switching waveform. Dead-time allows the previous MOSFET to turn off before switching the second MOSFET on thereby avoiding shoot-through. This is shown in Figure 6.4.1.



In addition to efficiency gains from removal of the schottky diode losses, synchronous rectification is the easiest method to implement the bi-directional current flow. Bi-directional converters have the ability to channel energy in both directions. Figure 6.4.2 shows the chosen converters with the diodes replaced by MOSFETs. The output sides of the converters are mirror images of the inputs, with no difference between the input and output circuitry as current could flow in both directions.

Lastly, the addition of bi-directional switching allows the converter to stay in CCM (continuous conduction mode) at light load. The converters have been designed to handle anything from the full 60Watts load of each PV module to loads approaching zero. In light load conditions, synchronous rectification allows the inductor current to reverse and avoids problems with the gain variation of the converter when it switches between discontinuous and continuous conduction modes. This gain change can significantly complicate the control loop and insert voltage swings during the transitions.

A schottky diode with a fast reverse recovery time can be added across the MOSFETs to improve the reverse recovery. The dead-time from the switching results in the MOSFETs sometimes becoming reversed biased and conducting. When the current changes direction the MOSFET continues to conduct for a short period called its reverse recovery. Losses are experienced in the converter during this period. If a schottky diode is placed in parallel to the MOSFET the schottky diode conducts the majority of the current when the MOSFET becomes reversed biased. This means a faster reverse recovery for the MOSFET, as the recovery time is proportional to the current it conducts.

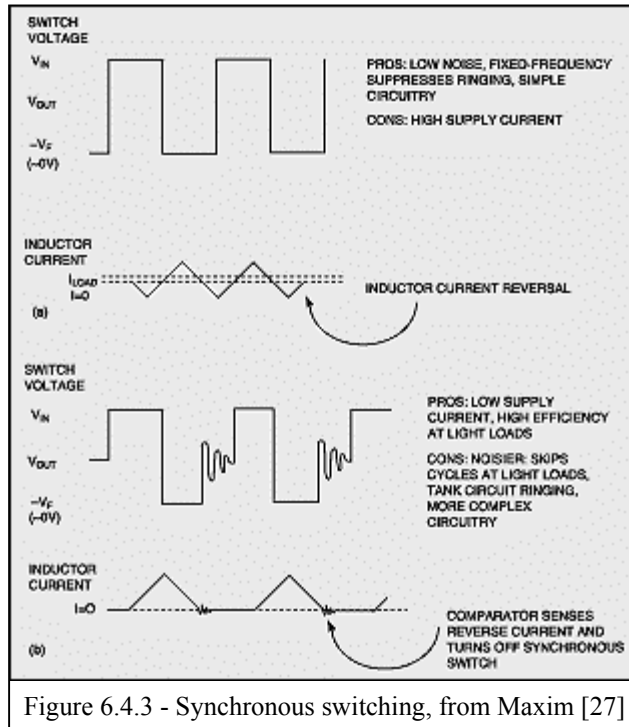


Figure 6.4.3 - Synchronous switching, from Maxim [27]

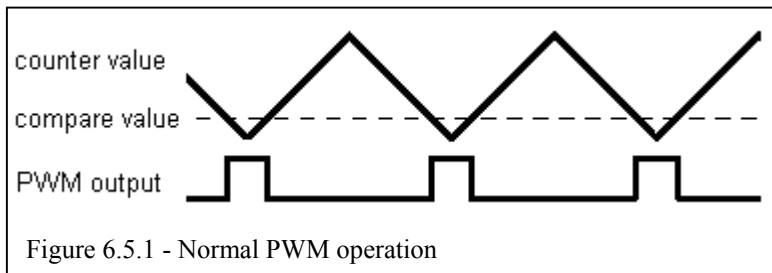
DCM (discontinuous conduction mode) operation can reduce efficiency of converters at medium load due to ringing caused by the sudden clamping of the inductor current. Figure 6.4.3 (b) shows the ringing generated by DCM, whereas Figure 6.4.3 (a) shows the relatively clean waveform of CCM. DCM also generates higher currents increasing the effects of parasitic losses. However, at loads significantly smaller than the inductor ripple for CCM, DCM operation is more efficient. At very light load, CCM operation with inductor current reversal has higher currents than DCM and causes energy to shuttle backwards and forwards through the converter losing some of this energy to parasitic losses [27].

## 6.5 Pulse Width Modulation

There are a number of ways to generate the pulse width modulation, PWM, shown in Figure 6.4.1, analogue circuitry, PWM chips, digital counters, and the timers on microcontrollers. As a microcontroller is already required in the design to perform the maximum power point tracking, using a microcontroller to generate the PWM represents a cheap solution that requires no additional hardware.

Many of the microcontrollers allowed for their timers to be used for PWM. For the switching required for synchronous rectification, two PWM channels that are in synchronization must be generated, with variable duty cycle. Furthermore, a switching frequency of 100kHz is desired for both converters. For the Cuk converter the fast switching frequency reduces the period of the inductor ripple and hence reduces the minimum inductor size. For the Flyback converter the fast switching reduces the minimum air gap of the transformer, as less energy must be stored in the air gap per switch cycle.

Normal PWM uses a counter that counts up and down between the maximum counter and zero [28]. This repeats itself continuously with each increment or decrement occurring at the clock frequency or a prescaled division of the clock frequency. A compare register is used to generate the PWM output from the counter. When the compare value matches the counter value a pin was set high if the counter is counting down, or low if the counter is counting up. This generated the PWM output as seen in Figure 6.5.1 and once started the PWM required no intervention from the microcontroller.

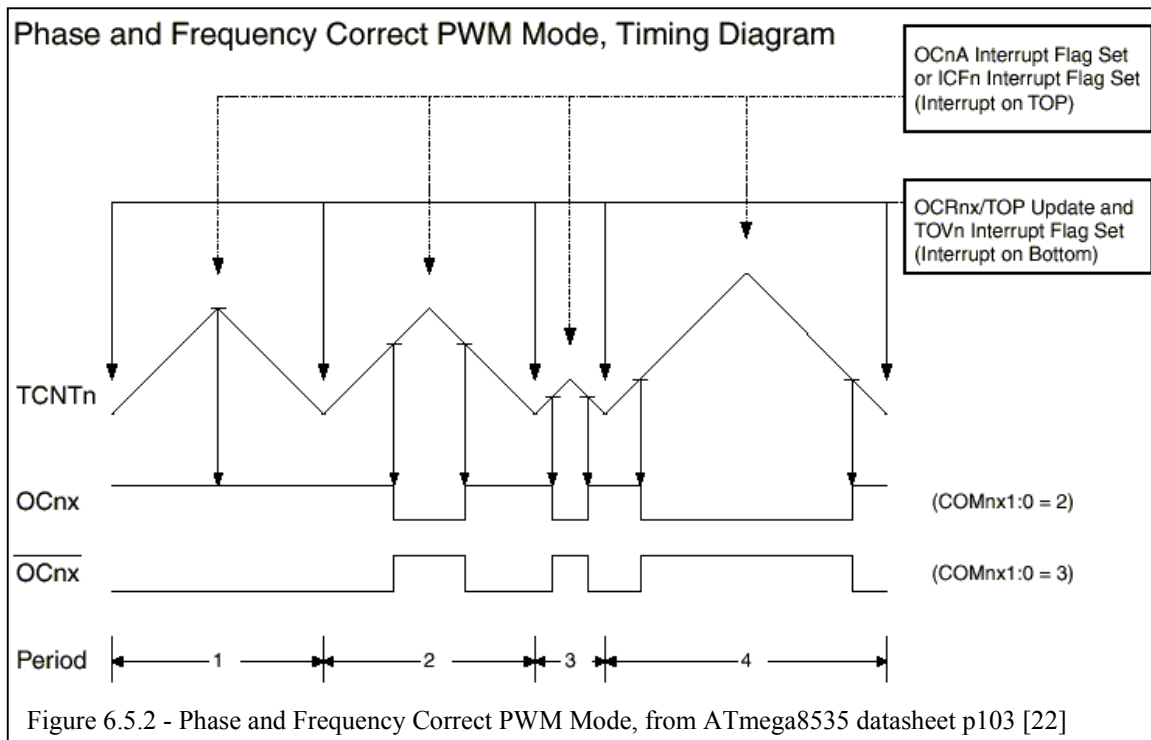


$$\text{Eq - 6.5.1} \quad f_{\max} = \frac{f_{clk}}{2 \times \text{CounterRange}}$$

The compare value sets the duty cycle of the PWM and the maximum frequency of the PWM can be derived as  $f_{\max}$ . A reasonable frequency is 8Mhz and the counter range for most microcontrollers is 8bits, 256. This creates a maximum frequency of 15.625kHz.

In the past only specialty chips such as the DSP were designed to generate phase and frequency correct PWM at frequencies as high as 100kHz. However, many of the newer chips have now addressed the problem of the PWM frequency.

Recently Phase and Frequency Correct PWM Mode was made available on many of the Atmel mega microcontrollers. This mode was similar to the normal PWM mode, however it allowed for variation in the range of the counter and hence allowed for precise frequency generation.



The Phase and Frequency Correct PWM Mode, shown in Figure 6.5.2, allows for a TOP value to be defined. The counter only counts up to the TOP value, instead of to its full range, before turning around and counting down again. This allows for the counter range to be changed and the PWM  $f_{max}$  is able to reach frequencies up to 100kHz while still able to perform variable duty cycle and remain in synchronization with a second PWM channel.

## 6.6 Driving the MOSFETs

Generating the PWM was only one step to switching the MOSFETs. A microcontroller is only able to supply currents of 20mA and this is insufficient to do hard switching of the MOSFETs. Hard switching refers to turning a MOSFET on and off as fast as possible. This reduces losses in the converter as less time is spent in the triode region (or linear region), where high currents and voltages are experienced by the MOSFET.

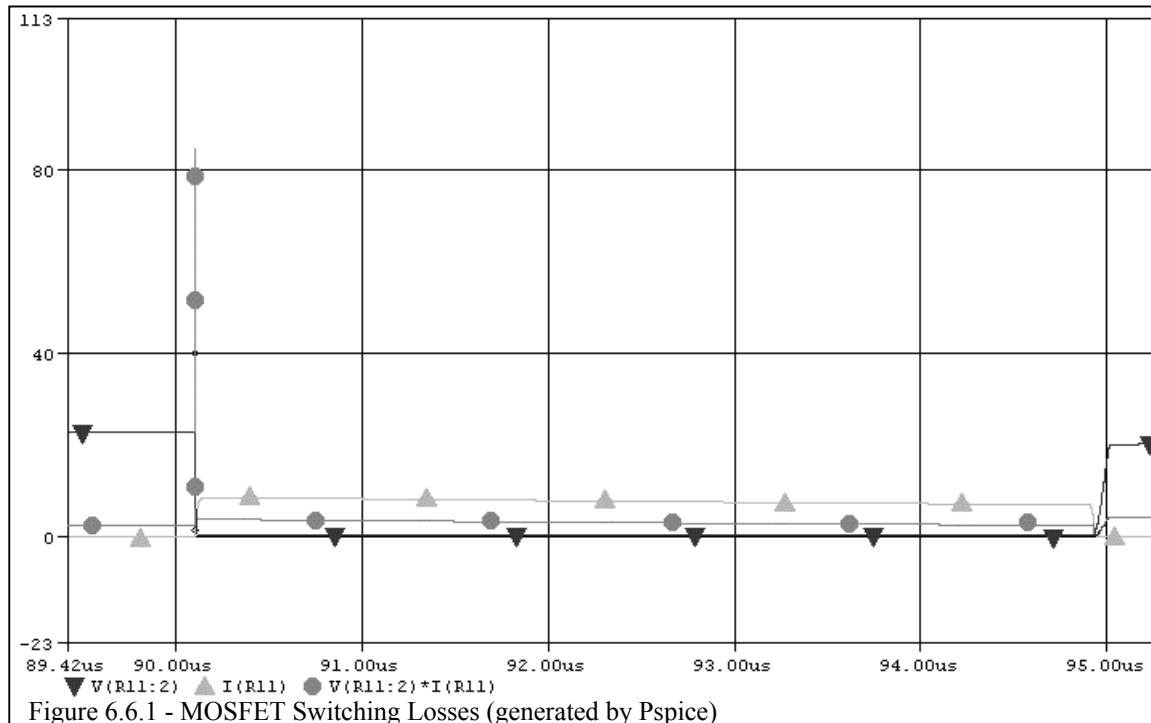


Figure 6.6.1 shows a Pspice demonstration of hard switching. Voltage, Current and power dissipation over the MOSFET are graphed. The large power dissipation spike shown when the MOSFET is switched on demonstrates the large losses experienced when the MOSFET is in the triode region. Hard switching significantly reduced this loss, as the period the large loss is experienced over is greatly reduced.

To perform hard switching of a MOSFET, current peaks of a few amps are required to charge and discharge the MOSFET. The charging and discharging only lasts a small fraction of the time so the average current is very small. MOSFETs that are in the power range of the converter have a maximum gate voltage of 16V. If this maximum gate voltage is exceeded, the metal oxide layer of the gate breaks down and the MOSFET acquires the attributes of a resistor. To switch the gate on, voltages above 6Volts are required for normal MOSFETs. Furthermore, the microcontroller outputs two 5V to 0V PWMs, so two channels are required.

Ideally a driver chips would be used that is TTL compatible (inputs of the driver can read 5V to 0V irrespective of the Vcc of the driver), and has internal regulation of the output between 7-12V.

However, no driver chips were found that met these specifications. The second best solution to driving the MOSFETs is using logic level MOSFETs that have a gate source turn on of about 3V and driving the MOSFETs with a driver drawing from the 5V regulator. With the  $V_{cc}$  of the driver chip at 5V, the inputs of the driver automatically becomes compatible with the microcontroller PWM and the problem of exceeding the maximum gate source voltage is avoided as the driver is running off the 5V regulator.

The Cuk converter is manipulated further to suit the Cascading Converter Topology shown in Figure 6.1.2. Figure 6.6.2 shows the new Cuk topology, where the positive terminal of the input is connected to the ground of the output.

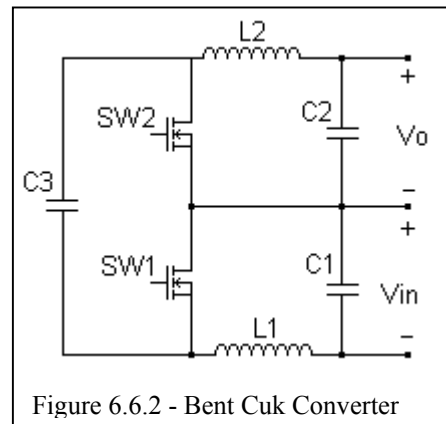


Figure 6.6.2 - Bent Cuk Converter

Figure 6.6.2 and Figure 6.4.2 (the Flyback converter), demonstrates that both converters have MOSFETs that are driven at different ground points. With separate ground points needed, isolation of one side must be implemented. There are two ways the isolated gate driving can be implemented, through either an optical or magnetic coupler, or a transformer.

The problem with the optical or magnetic coupler is driving circuitry is required at the other side of the coupler, as the large currents required to switch on the MOSFET can not be passed through the coupler. Additional driving circuitry at the other switch also requires a stable regulated power supply.

A transformer is able to directly transfer the high currents to the other side. However, the transformer removed the DC offset of the signal. This can be seen in Figure 6.6.3.

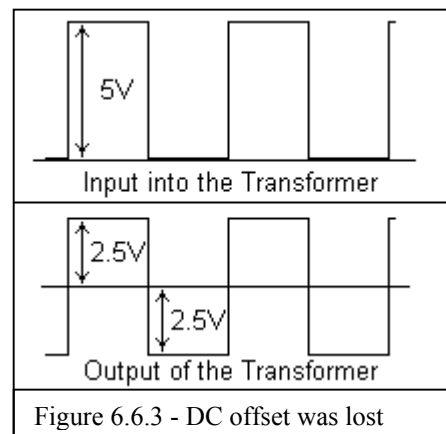


Figure 6.6.3 - DC offset was lost

The cheapest solution for isolated gate drive is implementation of a pulse transformer. A pulse transformer used a charge pump, diode and capacitor, to reconstitute the DC bias of a signal.

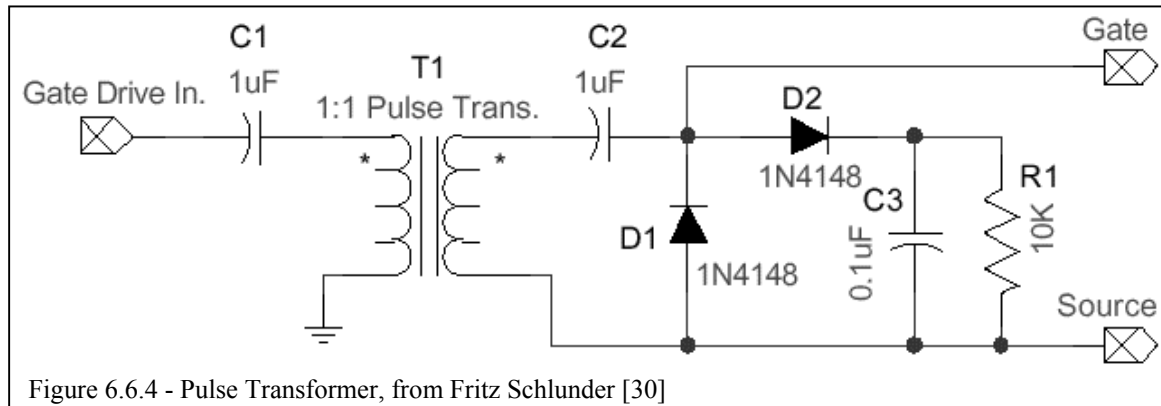


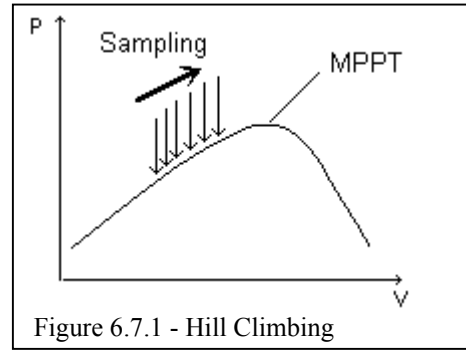
Figure 6.6.4 shows a Pulse Transformer. C2 and D1 form a charge pump that re-biased the output of the transformer. Testing and Pspice simulations show that the low of the output waveform is re-biased at 1V with the 1N4148 diode. This can pose a serious problem as logic level MOSFETs are being used and the fast turn off for hard switching can not be obtained with 1V. After analysis of the circuit, the 1V offset is attributed to the forward voltage drop of the diode. Therefore using schottky diodes, that have a very low forward voltage drop, the DC offset can be reduced to a tolerable level.

Another problem that the pulse transformer addressed is the effect of the inductance in the transformer. It can cause high voltage spikes on the output and if these are greater than 16V the metal oxide layer of the MOSFET gate can be punctured. To protect the gate a RCD snubber (resistor-capacitor-diode snubber) is added. R1, C3 and D2 in Figure 6.6.4, forming a snubber that reduces voltage spikes that can destroy the MOSFET.

## 6.7 Maximum Power Point Tracking

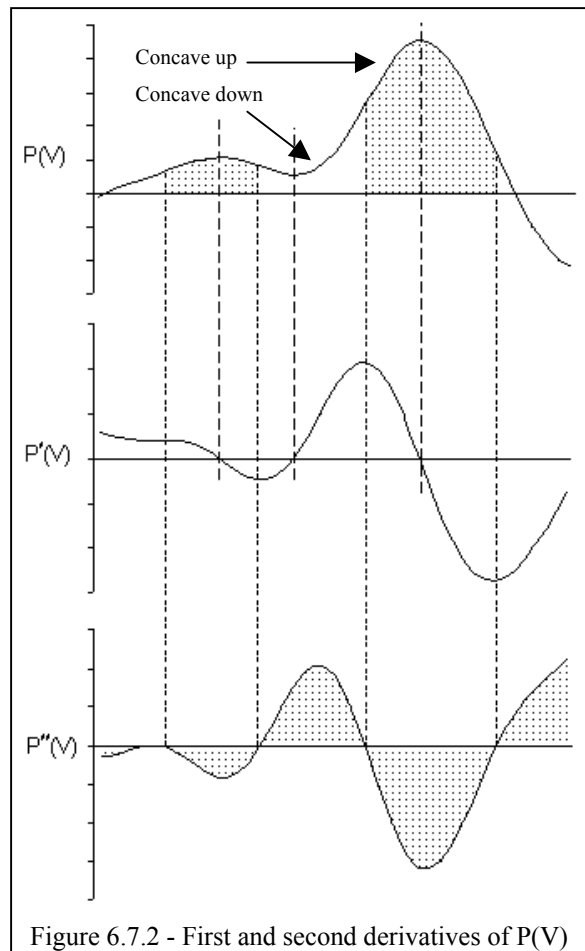
Maximum power point tracking is briefly explained in section 4.3 and the Perturb and Observe algorithm is mentioned as a simple tracking algorithm. It takes the voltage and the current from the PV module and finds the power output of the module. The duty cycle of the converter is then modified to get a slightly greater power output from the module.

The Perturb and Observe algorithm is a good starting point for the design for a maximum power point tracking algorithm. This algorithm uses the hill climbing technique demonstrated in Figure 6.7.1.



This algorithm can be greatly improved if the rate of climb is increased when the maximum power point is far away, and slowed when the MPPT reaches values near the maximum power point. In short a Slope Detection MPPT algorithm.

The gradient of the power voltage curve can be obtained from its derivative. Figure 6.7.2 shows an example power versus voltage function graphed in Excel.  $P'(V)$  is the derivative of the function and from the graph it becomes obvious that  $P'(V)$  is the gradient of the function. The further  $P'(V)$  is from zero, the faster the algorithm climbs to get to the MPP.



However, this fails when the power voltage function is near a local minima, a concave down [31]. The first derivative is close to zero in the concave down so rate of climb is very small. Calculating the second derivative,  $P''(V)$ , can solve this problem, as the second derivative is always positive in a concave down, and

negative in a concave up. The second derivative is the rate of change of the gradient, and the gradient change is always down for any hilltop.

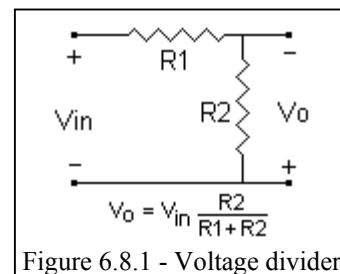
The main problem with this solution is that a basic Perturb and Observe algorithm is able to perform two or three adjustments of the duty in the time it took for this algorithm to make one adjustment.

However, this is offset a increased maximum power point seeking speed when the operating point of a PV module is far away from the maximum power point. The MPPT is able to reach a point near MPP faster even though it may reach the exact MPP slower. Furthermore, the nature of the algorithm allows for the MPPT to switch to a fine adjustment mode when the PV module is very close to its MPP. This allows for higher accuracy than the Perturb and Observe at the MPP. Finally the increased delay between samples of the voltage and current reduces the possible instability in the feedback loop.

## 6.8 Current and Voltage Sensing

The ADC of microcontrollers vary between their GND and Vcc. As microcontrollers generally operate with a Vcc of 5V, the analogue input voltages to the microcontroller vary between 0V to 5V for the current and voltage sensors.

For the voltage sensor the expected range of its operation is 5V to 20V. If the voltage falls below 5V the microcontroller does not work reliably, and 20V is the maximum open loop voltage for the PV modules (see section 5.1). This is as simple as a voltage divider, shown in Figure 6.8.1.



The input resistance of the microcontroller is in the  $2 \times 10^6 \Omega$  range, and this resistance is placed in parallel to R2. To prevent this extra resistance from causing significant error the resistor R2 is smaller than 20k for a possible 1% error when  $2M\Omega$  is placed in parallel. Having R2 and R1 too small means the voltage sensor can cause too much of a power drain.

The current sensor is not as simple. The ADC of the microcontroller only measures voltages so the current must be converted into a voltage reading. This is done using an extremely small resistance in series with the PV module. Using Ohms law, voltage equals resistance multiplied by current, the current is found from the small resistor and the voltage measured over the resistor.

The resistance used is small enough that the power loss over the resistor is small. However, this means the voltage to be read is extremely small too. An amplifier is required to amplify the voltage over the resistor so a reasonable number range can be read from the ADC. The main problem with amplifying very small voltage signals are slight differences between the ground of what is being measured and the ground of the sensor. This causes large DC offsets in the output of the amplifier.

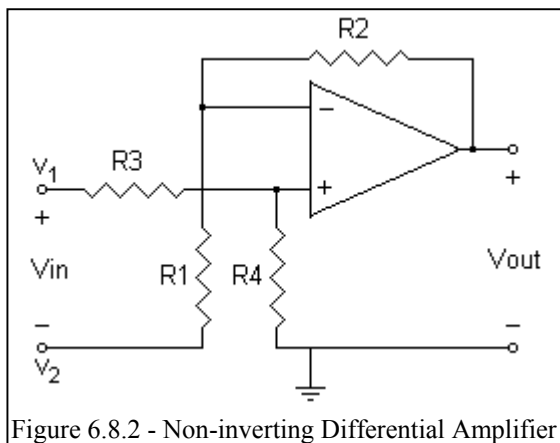


Figure 6.8.2 - Non-inverting Differential Amplifier

A non-inverting differential amplifier is used (Figure 6.8.2), as it had a high common-mode rejection ratio (CMRR). CMRR is defined as the ratio of the differential gain of an amplifier to the common-mode gain. To explain simply, the amplifier specifically increases the voltage difference between the two input voltages, and reduces the DC bias of the two input voltages.

This is especially useful when the ground of the  $V_{in}$  has a slight offset and the amplifier could amplify this offset. A small resistance in the PCB tracks, creates slight voltage differences in the ground, and often causes this slight offset. A good ground plane can reduce this effect, but the addition of the differential amplifier further improves the current sensing.

Steven R. Shaw shows the derivation of Equation 6.8.1 for the output of a differential amp [32]. If  $R_4$  is made equal to  $R_2$  and  $R_3$  is made equal to  $R_1$ , the equation from Shaw can be simplified to give an amplified output completely dependent on the voltage difference between  $V_2$  and  $V_1$ , Equation 6.8.2. The amplification can then be set by the ratio of  $R_2$  and  $R_1$ .

Eq - 6.8.1 obtained from Shaw [32]

$$V_o = \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} V_2 - \frac{R_2}{R_1} V_1$$

Sub in  $R_4 = R_2$ , and  $R_3 = R_1$

$$V_o = \left(1 + \frac{R_2}{R_1}\right) \frac{R_2}{R_1 + R_2} V_2 - \frac{R_2}{R_1} V_1$$

$$V_o = \frac{R_2}{R_1} \left( \left(\frac{R_1}{R_2} + 1\right) \frac{R_2}{R_1 + R_2} V_2 - V_1 \right)$$

$$V_o = \frac{R_2}{R_1} \left( \left(\frac{R_1}{R_1 + R_2} + \frac{R_2}{R_1 + R_2}\right) V_2 - V_1 \right)$$

$$V_o = \frac{R_2}{R_1} (V_2 - V_1) \quad \text{Eq - 6.8.2}$$

## 6.9 Finalised Block Diagram

With most of the interdependencies of the design resolved, the block diagram of the hardware is completed (Figure 6.9.1).

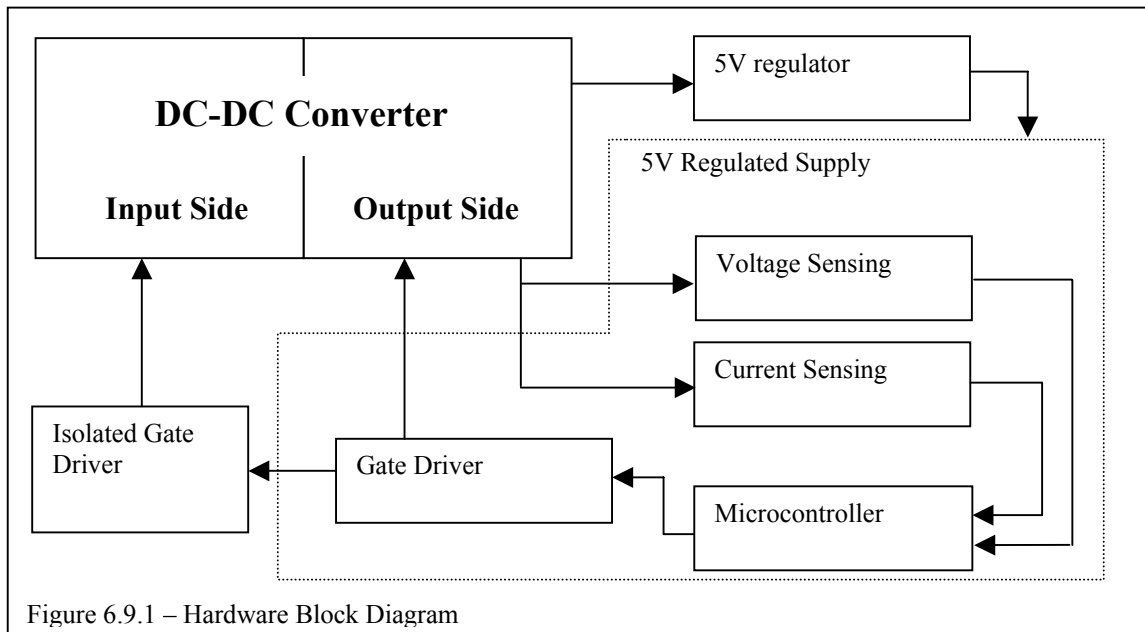


Figure 6.9.1 – Hardware Block Diagram

# 7.0 Implementation

## 7.1 Cuk Converter

Analysis of the Cuk converter, Figure 7.1.1, was covered first, as it was the main converter in the design. There were three component values that needed to be calculated, the input capacitor, the input inductor and the centre capacitor. As the output of the converter had the same specifications as the input, the output capacitor and output inductor mirrored the inputs.

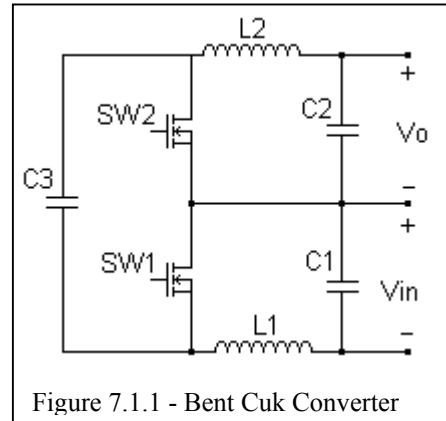


Figure 7.1.1 - Bent Cuk Converter

There were two modes a switch mode converter operated in, CCM and DCM. Figure 7.1.2 showed continuous conduction mode (CCM), where the current in the inductor increased and decreased, but not entirely stop. With discontinuous conduction mode (DCM), Figure 7.1.3, the current in the inductor always returned to zero each switching cycle.

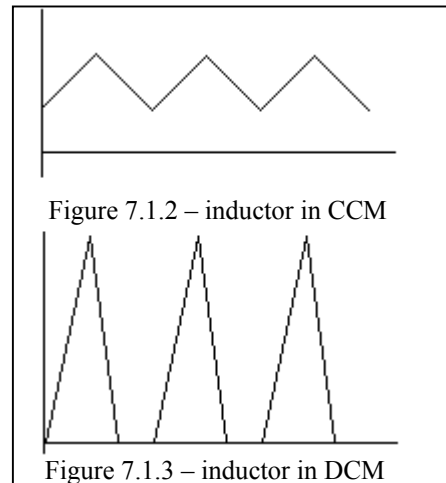


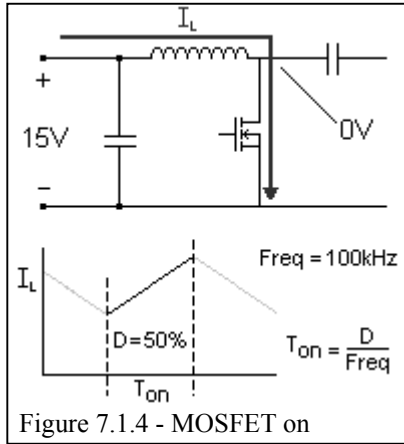
Figure 7.1.2 – inductor in CCM

Figure 7.1.3 – inductor in DCM

The inductor was chosen as the starting point. It was decided that the converter would operate in continuous conduction mode. Continuous conduction mode lowered the peak currents flowing through the inductor, and consequently reduced the losses in the converter.

With a maximum current of 4Amps expected a suitable maximum current ripple,  $\Delta i$ , of 1A was chosen. The equation 7.1.1 was for the voltage over an inductor. The MOSFET on cycle was chosen for analysis. MOSFET on and MOSFET off cycles were complementary, so analysing either gave the same answer for the inductor size.

$$\text{Eq - 7.1.1} \quad V_L = L \frac{\Delta i}{\Delta t}$$



$$\Delta i = 1A$$

$$V_L = 15V$$

$$\Delta t = \frac{D}{f} = \frac{0.5}{100kHz} = 5 \times 10^{-6} s$$

Sub in values into equation 7.1.1

$$V_L = L \frac{\Delta i}{\Delta t}$$

$$L = V_L \frac{\Delta t}{\Delta i}$$

$$L = 15 \frac{5 \times 10^{-6}}{1} = 75 \mu H$$

Figure 7.1.4 shows the characteristics of the converter during the input MOSFETs on cycle. It was assumed that the input was 15V and there was duty cycle of 50%.

When the MOSFET was on,  $V_L$  was equal to the input voltage, as there was negligible voltage over the MOSFET. The on cycle,  $T_{on}$ , is shown in Figure 7.14 was found from the duty cycle and the inverse of the frequency.

This gave an inductor size of  $75\mu H$ , which was rounded up to  $100\mu H$ . A maximum rating of 4A DC was required. So  $100\mu H$  1400 Series Bobbin inductors from Newport Components were chosen from Farnell [33]. The ones chosen had 5.4A max DC rating and a maximum resistance of  $0.042\Omega$ .

Knowing there was a maximum current ripple of 1A at the input, the input capacitor was calculated. There were two considerations, firstly the capacitor was used to limit the input voltage ripple, and secondly the input capacitor took a 1A current ripple.

Figure 7.1.5 shows the capacitor charging. The input voltage ripple was calculated from the charge that was stored in the capacitor. The charge stored was derived from the maximum current ripple,  $I_{p-p}$ , of 1A.

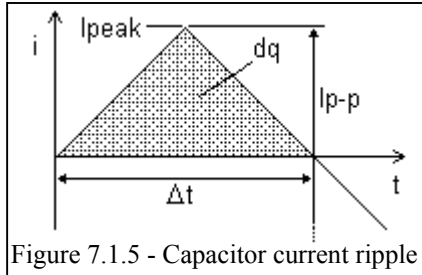


Figure 7.1.5 - Capacitor current ripple

$$I_{peak} = \frac{1}{2} I_{p-p} = 0.5 A$$

$$\Delta t = \frac{1}{2f} = \frac{1}{2 \cdot 100 kHz} = 5 \times 10^{-6} s$$

$$dq = \int i \cdot dt \quad \text{Eq - 7.1.2}$$

$$dq = \frac{1}{2} I_{peak} \cdot \Delta t$$

$$dq = 1.25 \mu C$$

The standard current equations 7.1.3 and 7.1.4 were combined to give equation 7.1.5, which showed the relationship between the charge on a capacitor and the voltage.

$$i = C \frac{dv}{dt} \quad \text{Eq - 7.1.3} \quad i = \frac{dq}{dt} \quad \text{Eq - 7.1.4}$$

$$dq = C \cdot dv \quad \text{Eq - 7.1.5}$$

A maximum voltage ripple of 1% was specified for the input capacitor. With an input voltage of 15V this was 0.15V for the input ripple. The charge that was stored in the capacitor was dq 1.25μC. Using equation 7.1.5 a minimum capacitor size of 8.3μF was needed to regulate the input ripple to 1%.

Eq - 7.1.6 from Erickson A1.9 [19]

$$I_{rms} = \frac{\Delta i}{\sqrt{3}}$$

The input capacitor was also designed to handle a peak to peak current ripple of 1A ( $\Delta i = i_{pp}/2 = 0.5A$ ). This required a significantly larger capacitor. Figure 7.1.2 shows the inductor current waveform in CCM. The RMS current equation from Erickson for the CCM waveform was equation 7.1.6. This gave a RMS ripple of 0.289A. A 220uF 50V 1.37A ZL High Current Ultra Low Impedance capacitor was chosen from Farnell [33].

The centre capacitor of the Cuk converter had a number of specifications that were met. The capacitor was large enough that when the inductor current charged the capacitor, the capacitor did not cause a significant voltage decrease over the inductor. The capacitor could also withstand the maximum converter current passing through it and the sum of the input and output voltages.

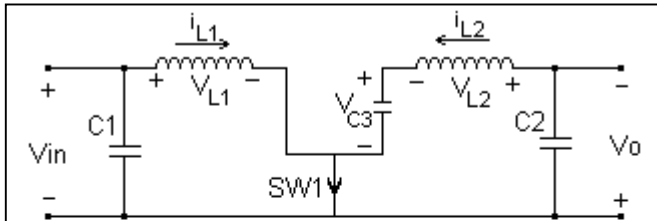


Figure 7.1.6 – Cuk converter, SW1 on and SW2 off

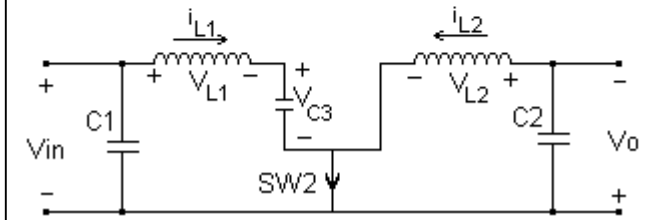


Figure 7.1.7 – Cuk converter, SW1 off and SW2 on

Figure 7.1.6 and 7.1.7 shows how the charging and discharging of  $C_3$  caused a voltage  $V_{C3}$ , which affected the inductor voltages and hence inductor currents. The change in  $V_{C3}$  was small otherwise the charging of  $C_3$  significantly reduced the inductor currents.

$$\Delta V_{C3} = \frac{1}{C} \int_0^{(1-D)T_s} i_{L1} dt$$

The equation and derivation for the change in  $V_{C3}$ , equation 7.1.7, was obtained from M.U.R. [34].

It was assumed that the  $i_{L1}$  had minimal ripple and there was a maximum current of 4A.  $T_s = 1/100\text{kHz}$ , and the duty cycle was 50%. These values were used with equation 7.1.6 to obtain the minimum capacitor for a 10% error caused by  $\Delta V_{C3}$ .

$\Delta V_{C3} = V_{in} \cdot 10\% = 15 \times 0.10 = 1.5V$	$\Delta V_{C3} \cdot C = \int_0^{(1-D)T_s} i_{L1} dt$
$T_s = \frac{1}{100 kHz} = 10 \mu S$	$C = \frac{1}{\Delta V_{C3}} (-i_{L1} \cdot (1-D)T_s)$
$i_{L1} = 4A$	$C = \frac{1}{1.5} (4 \times 5 \mu S)$
$D = 50\% = 0.5$	$C = 13.33 \mu F$

A 10% error in  $\Delta V_{C3}$  required a capacitor of size 13.33 $\mu$ F. However, Pspice simulations revealed that at 4Amps load, 4A RMS current rating was required of the capacitor. Three of the 220uF 50V 1.37A capacitors that were mentioned earlier were put in parallel. This gave a maximum of 4.11A RMS combined.

The highest voltage these capacitors were subjected to was  $V_{in} + V_o$ .  $V_{in}$  and  $V_o$  have maximums of 20V each so a maximum of 40V was seen over C3. This was below the 50V rating of the capacitors.

## 7.2 Flyback Converter

The Flyback converter is shown in Figure 7.2.1. The most important part of the Flyback converter was the transformer. The transformer design detailed in section 6.3 was used to choose a transformer and calculate the turns.

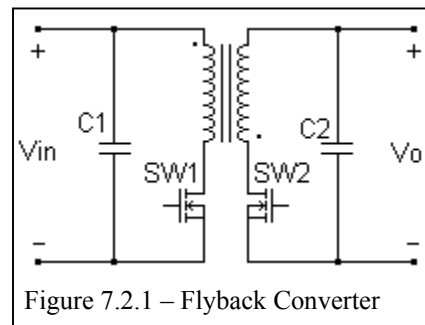


Figure 7.2.1 – Flyback Converter

An EFD25 transformer was chosen by elimination. The smallest ETD (ETD29) was 25.4 mm high [35], while maximum clearance above the PCB was 22mm (from section 5.1). A planar core looked impressive, but was difficult for prototype construction, and from calculations it was too small to handle the power requirements without significant losses. Several different transformer cores were tested for suitability with the transformer design procedure in section 6.3. The EFD25 came out as the best compromise between core size and power handling.

effective volume ( $V_e$ )	= 3300mm <sup>3</sup>
effective length ( $l_e$ )	= 57.0mm
effective area ( $A_e$ )	= 58.0mm <sup>2</sup>
minimum area ( $A_{min}$ )	= 55.0mm <sup>2</sup>
permeability of N87 ( $\mu_e$ or $\mu_r$ )	=1440 N/A <sup>2</sup>

The EFD25 had the specifications, shown above, that were obtained from the Ferroxcube website [36].

$$\text{Eq - 7.2.1} \quad l_a = \frac{P 2 \mu_0}{B^2 A_e f}$$

Combining equations 6.3.1, 6.3.2, 6.3.3, and 6.3.4, resulted in equation 7.2.1 for the minimum air gap.

The only core material available for the EFD25 at Farnell was the N87 material type. This had a maximum flux saturation ( $B_{sat}$ ) of 480mT [37]. At the maximum power,  $B = 480\text{mT}$  was designed for. The flux is always less than 480mT due to losses in the converter and the core. The power ( $P$ ) the transformer was designed to handle was 60Watts specified in section 5.1. The permeability of free space ( $\mu_0$ ) was found from Tipler [22] to be  $4\pi \cdot 10^{-7}$  N/A<sup>2</sup>. The frequency ( $f$ ) chosen in section 6.5 was 100kHz.

$$l_a = \frac{60 \cdot 2 \cdot 4\pi \cdot 10^{-7}}{(0.48)^2 \cdot 58 \cdot 10^{-6} \cdot 100000}$$

$$l_a = 0.1128 \text{ mm}$$

The above values were substituted into equation 7.2.1, to give a minimum air gap of 0.1128mm. The air gap was inserted between two half cores of the transformer, so the air gap cut the transformer twice. Hence, a 0.0564mm gap between the two half cores was

effectively a 0.1128mm gap. An effective air gap of 0.2mm was chosen as 0.113mm generated too few turns on the transformer in subsequent steps.

To find the maximum turns of the transformer the reluctance of the core,  $\mathfrak{R}$ , and the  $I_{\text{peak}}$  current was calculated. From section 6.3 it was known that the Flyback generated  $I_{\text{peak}}$  currents four times the average current through the converter.

$$\mathfrak{R} = \frac{l_e}{\mu_r \mu_0 A_e} + \frac{l_a}{\mu_0 A_e}$$

Sub in the values already defined previously in this section

$$\mathfrak{R} = \frac{1}{\mu_0 A_e} \left( \frac{l_e}{\mu_r} + l_a \right)$$

$$\mathfrak{R} = \frac{1}{4\pi \cdot 10^{-7} \cdot 58 \cdot 10^{-6}} \left( \frac{0.057}{1440} + 0.0002 \right)$$

$$\mathfrak{R} = 3.287 \cdot 10^6 \text{ per Henry}$$

The maximum current the PV module was able to produce was 4A. However, 4Amps was in short circuit conditions where the converter was unable to operate in due to lack of voltage. The transformer generally operated in much lighter load, and biasing the transformer to a heavier load than what it would ever encounter generates significant losses from leakage inductance. So the maximum operation current of the transformer was set at 3A with  $I_{\text{peak}}=12\text{A}$ .

The reluctance of the core,  $\mathfrak{R}$ , was calculated with equation 6.3.6, giving  $3.287 \times 10^6$  per Henry.

After the  $I_{\text{peak}}$  and  $\mathfrak{R}$  were calculated the maximum turns for the primary was obtained using equation 6.3.5.

$$N = \frac{\mathfrak{R} B_{sat} A_e}{I_{peak}}$$

$$N = \frac{3.287 \cdot 10^6 \cdot 0.48 \cdot 58 \cdot 10^{-6}}{12}$$

$$N = 7.63$$

This gave a maximum of 7 primary turns, as the value must be rounded down. The maximum number of turns was used as a greater number of turns improved efficiency. The secondary had the same number of turns as no voltage step up or step down was required. Section 6.1 explained how the input and output voltages of the converters were always closely matched.

Capacitors were required in the Flyback to prevent the high ripple currents and voltages from adversely affecting the input and output.

Section 7.1 calculated the required input and output capacitor sizes for the Cuk. The procedure for the Flyback did not differ greatly. The Flyback had a peak output and input current of 12A compared to the 0.5A of the Cuk converter. Equations 7.1.2 and 7.1.5 were analysed and if the  $I_{peak}$  was increased by 24 then the required capacitor size was increased the same amount. So for the Flyback to achieve a maximum of 1% ripple in its inputs and outputs, a capacitor 24 times the 8.3 $\mu$ F required by the Cuk converter was needed. A minimum capacitor size of 199 $\mu$ F for the capacitors of the Flyback was required to achieve a maximum of 1% voltage ripple.

The Flyback converter was simulated with a load of 3A and the RMS current ripple was found to be 4A. Three of the 220 $\mu$ F 50V 1.37A capacitors that were mentioned earlier were put in parallel. This gave a maximum of 4.11A RMS combined.

### 7.3 Switching Circuitry

Section 6.6 explained the basics of the switching circuitry. The MOSFETs were hard switched to reduce MOSFET losses. A driver chip was used with a  $V_{cc}$  of 5V to allow for microcontroller inputs and to prevent exceeding the gate source voltage limit of the MOSFET. Logic level MOSFETs were used to allow for the low output voltage of the driver chip. Finally isolation was implemented on one side with a pulse transformer.

The characteristics of several MOSFETs were tabulated (see Appendix B). From the MOSFET table, the IRLZ series of MOSFETs was shown to be most suitable. They met the required current and voltage ratings required (section 5.1). Furthermore, they had better efficiency, with low forward resistance, and low gate charge, which meant faster switching with fewer losses.

The IRLZ24N was initially chosen for its low cost. While the IRLZ44N and IRLZ34N had lower on resistances, which resulted in lower on losses, the IRLZ24N had a smaller gate charge and switched faster reducing the switching losses. The ratio of the forward conduction losses and the switching losses, determined the best MOSFET for the application. Deciding which was best required some initial calculations backed with hardware test results.

The driver chip chosen was the TPS2812 [38]. It had two non-inverting channels with 2A peak output current. The inputs were CMOS, but the chip was using the 5V regulated supply so the inputs were compatible with the microcontroller. As the driver chip may drain significant pulses of power from the 5V regulator, a 47 $\mu$ F capacitor was placed at the  $V_{cc}$  of the driver chip to keep the 5V regulated supply stable and ensure the microcontroller was not affected by possible voltage ripple generated by the driver.

The design of the pulse transformer was as described in section 6.6. The schottky diode used in the pulse transformer was the 1N5817, which had the lowest forward drop of the diodes researched in Appendix C.

Finally, schottky diodes were placed in parallel to the MOSFETs, which gave improved reverse recovery and allowed for higher efficiency in single side switching if bi-directional switching was not required. The 1N5822 was chosen as it had a relatively low forward drop, while being able to handle same currents and voltages as the MOSFETs

Figure 7.3.1 shows the implementation of the switching circuitry.

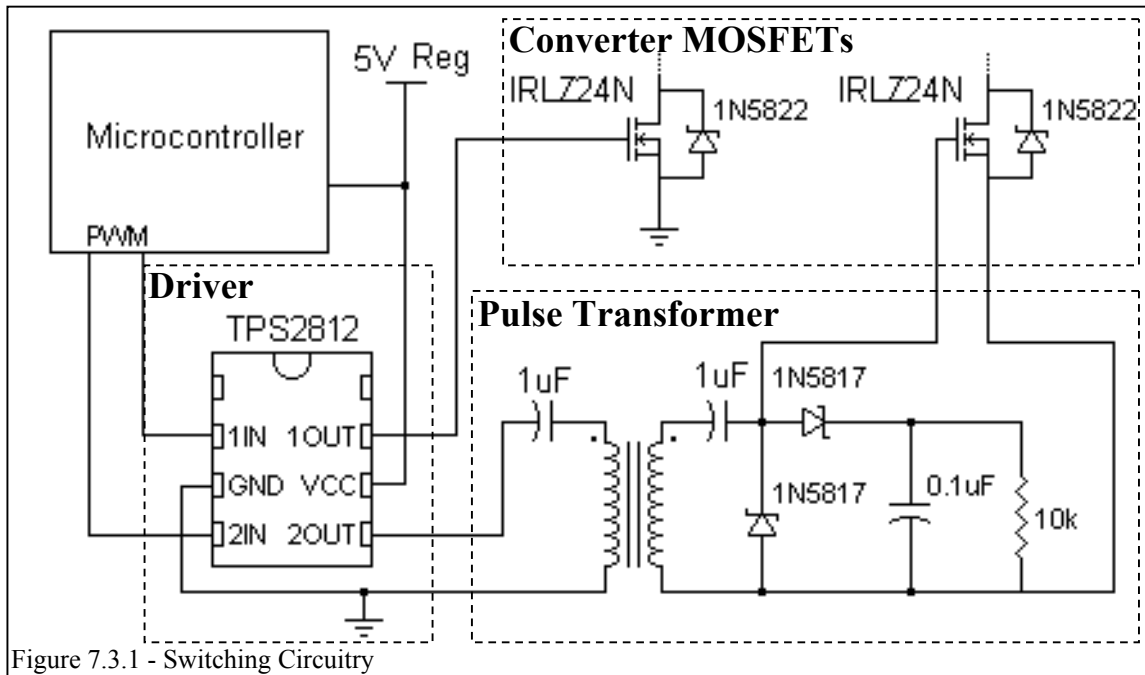


Figure 7.3.1 - Switching Circuitry

## 7.4 Sensing Circuitry

Section 6.8 explained the calculations and hardware required to perform the current and voltage sensing. All that remained was to choose suitable components.

The voltage divider was described in Figure 6.8.1. By setting  $R_1$  to 33k and  $R_2$  to 11k, the voltage was reduced by 4 from 0V-20V, to 0V-5V. When  $R_2$  was placed in parallel with the 2M $\Omega$  of the microcontroller input, the effective resistance was 10.94k $\Omega$ . This was only a 0.55% variation from 11k and was negligible.

$$V_o = V_{in} \frac{R_2}{R_1 + R_2}$$

$$V_o = V_{in} \frac{11k}{33k + 11k}$$

$$V_o = \frac{1}{4} V_{in}$$

A  $0.02\Omega$  current sensing resistor was placed in series with the PV module to measure the current. For the maximum current 4A, it generated 0.08V. A non-inverting differential amp was used to increase this voltage to a level where the microcontroller's analogue to digital converter was easily able to read the value. The differential amp can be seen in Figure 6.8.2. The easily obtainable LM358 was chosen for the op amp.

Equation 6.8.2 shows that the amplification of the differential amp was directly proportional to  $R_2/R_1$ .  $R_2$  was set to 120k and  $R_1$  to 3k and gave an amplification of 40. This amplified the 0.08V at 4A over the current sensing resistor to 3.2V.

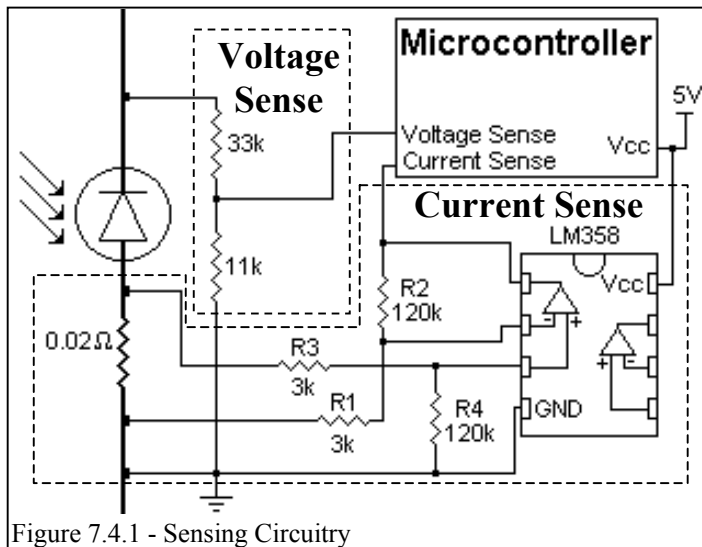


Figure 7.4.1 - Sensing Circuitry

Figure 7.4.1 shows the implemented hardware for the voltage and current sensing.

## 7.5 Microcontroller

The microcontroller chosen was the ATmega8535. This microcontroller had the Phase and Frequency Correct PWM mode, and eight channels multiplexed to an 8-bit analogue to digital converter. Timer1 of the microcontroller allowed for direct PWM control of two output pins, ideal for generating synchronous rectification. Atmels also have a reputation for being a particularly study microcontroller.

The ATmega8535 was unobtainable, so the AT90S8535 was to be used until the ATmega8535 becomes available. The AT90S8535 had similar pin configuration to the

ATmega8535, but was unable to generate the 100kHz PWM easily with the 8MHz crystal that was chosen.

## **7.6 Completed Hardware Design**

The Protel schematic and PCBs can be found in Appendix D and E respectively. For the final design eleven Cuk converters and one Flyback will be required to MPPT the 12 solar panels. In the early stage of this project, two Cuk converters and one Flyback was sufficient for development.

## **7.7 Microcontroller Code**

The ATmega8535 was not available as it is a relatively new chip. Without the ATmega8535, a different method to generate the PWM was engineered. This was a temporary solution as the ATmega8535 should be obtainable in the near future, so the explanation on how the switching was achieved will be brief.

The synchronous PWM was done using the interrupts of Timer1, and directly driving pins from the interrupt routine. The AVR GCC C compiler [39] was used to compile c code into assembly. Adjustments were then made to the generated assembly code to increase the speed. This gave a reasonably efficient PWM with a variable duty cycle, 21% to 84% (from tests), and 30% of the microcontroller clock cycles were spent generating the PWM. The duty cycle was adjustable using the interrupt pins. This complicated compile process was necessary as the c compiler inserted a high overhead with its inefficient code. If the generated assembly code was used, the duty was limited between 40% to 60% due to interrupt routine delays and 80% of the clock cycles were spent switching. The majority of these delays were from pushing and popping registers in the interrupt routine. These delays were removed with smart assembly code.

Once the PWM was completed, simple MPPT code was generated. The algorithm used was Perturb and Observe. The duty of the PWM is adjusted and depending on whether this generated an increase in the output power or a decrease in the output power the duty cycle will adjust. This performed 25 current analogue to digital conversions and 25

voltage analogue to digital conversions between each duty cycle adjustment. The ADC clock frequency was set at 62.5kHz and each conversion takes 25 ADC clock cycles. This gives 2500 ADC conversions per second, or 50 adjustments of the PWM every each second.

Appendix F shows the c code and how to adjusted the generated assembly code.

## 8.0 Results and discussion

### 8.1 Theoretical Calculations

#### 8.1.1 Converters in Idle State

The power consumption of the converter when idle should not drain a significant portion of the energy from the PV module. To ensure that the converter does adversely affect the power output of the module, the power consumption of the microcontroller, sensing circuitry and the driver chip in idle state were calculated with the assumption that the PV module was generating 15V and 3A.

According to the AT90S8535 datasheet [28], the microcontroller drained 6.4mA at 4MHz and 3V. The microcontroller in the design was running at 8Mhz and 5V. The power consumption was doubled as microcontrollers use CMOS technology and power was only lost with CMOS when switching. So doubling the clock frequency doubled the power consumption. The difference in current consumption due to the voltage was negligible. Hence, the microcontroller used 12.8mA at 5V, 64mW of power.

The driver chip in idle state used 5 $\mu$ A of current. At 5V this resulted in 25 $\mu$ W of power consumption.

The voltage sensor was a series combination of resistors 11k and 33k, and the voltage of the panel (15V) was placed over these resistors. Power is  $V^2/R$ , so the voltage sensor used 5.11mW of power.

The 0.02 $\Omega$  current sense resistor had 3A passing through it. Power is  $I^2R$ , so the current sensor dissipated 180mW.

The differential amp had losses in the resistors and the op amp. The op amp had a 500 $\mu$ A static drain at 5V. So 2.5mW was dissipated in the op amp. Analysis of the resistors used in the differential amp Figure 6.8.2, revealed R3 and R4 experienced the voltage over the 0.02 current sensor, 0.06V. This was negligible since R3 and R4 in series was 123k $\Omega$ . R1

and R2 experienced  $40 \times 0.06V$ , or 2.4V, over them. R1 and R2 was  $123k\Omega$  so  $46.8\mu W$  was dissipated. In total 2.55mW dissipated in the differential amp.

Finally the 5V regulator had an input of 15V and an output of 5V while supplying the same current it drained. Consequently, anything that the 5V regulator supplies, incurred double its power consumption as losses in the regulator. The regulator supplied the amplifier, microcontroller and driver chip. Their combined power consumption was  $2.55mW + 25\mu W + 64mW = 66.6mW$ , and the corresponding loss in the regulator was 133.2mW

Table 8.1.1.1 - Idle State Losses

Component	Loss (mW)
Micrcontroller	64
Driver Chip	0.025
Voltage Sensor	5.11
Current Sensor	180
Differential Amp	2.55
5V Regulator	133.2
Total	385

At 15V 3A the solar panel was generating 45W. Table 8.1.1.1 shows the power consumed when the converter was not switching. The percentage of power the circuitry used when idle was  $0.385/45$ , 0.86% of the generated power. Less than 1% power was deemed acceptable for the design.

### 8.1.2 MOSFET Gate switching Losses

The energy required for charging and discharging the gates of the MOSFETs was most easily determined by considering the gate as a capacitor. The gate capacitance for the IRLZ24N was 15nC (Appendix B), and the formula for the power dissipation was given by  $W = c\varepsilon^2$  (p814 Tipler [22]). This was simplified to  $E = CV^2$  for each charge and discharge. The assumption was made that the gate fully charges before discharging. With  $C = 15nC$  and voltage over the gate at 5V the energy dissipated was 375nJoules. This was multiplied by the switching frequency of 100kHz and gave 37.5mW per switch. For synchronous switching this was 75mW. As the 5V Regulator supplied the driver there

was a 150mW increase in regulator power dissipation. So a total of 225mW was consumed in switching the MOSFETs.

### 8.1.3 Cuk Converter

The power loss for the Cuk Converter was found for 3A with a 0.5A  $\Delta i$  inductor ripple and a 50% duty cycle, section 7.1 explains these assumptions.

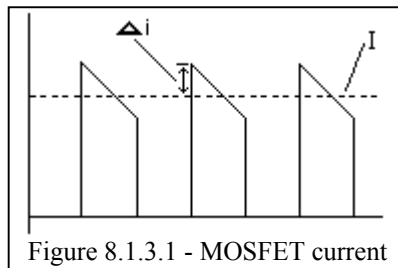
The inductor chosen had a 0.042 $\Omega$  resistance. Using the DC plus linear ripple, equation 8.1.3.1 the RMS current through the inductor was calculated. The inductor current waveform can be seen in Figure 7.1.2.

Eq - 8.1.3.1 from Erickson A1.2 [19]

$$I_{rms} = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2}$$

This gave 3.014A RMS through the inductor, and this created a power loss of 0.382W per inductor, or a combined 763mW loss for the inductors.

The MOSFETs also had a loss when conducting. The current through the MOSFET when it was conducting was the combined inductor current and the capacitor discharge current. This was shown in Figure 8.1.3.1. Assuming 50% duty cycle the MOSFET current waveform had an on current double the average converter current ( $I = 6A$ ) and  $\Delta i$  double the ripple seen in the inductor ( $\Delta i = 1A$ ).



Eq - 8.1.3.2 from Erickson A1.6 [19]

$$I_{rms} = I \sqrt{D} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2}$$

Equation 8.1.3.2 gave 3.014A RMS through the MOSFET, which had a  $R_{on}$  of 0.06 (Appendix B). This gave 545mW dissipated per MOSFET, or 1090mW for both MOSFETs.

There were two other major losses that were too complex to justify theoretical calculation, the switching losses and the ESR (equivalent series resistance) losses of the capacitors.

Table 8.1.3.2 – Cuk Converter Losses

Component	Loss (mW)
Idle State Losses	385
MOSFET Gate Charge Losses	225
Inductor Losses	763
MOSFET On Resistance Losses	1090
MOSFET Switching Losses	?
Capacitor ESR Losses	?
Total	2463

The expected power dissipation of the Cuk converter was expected to be 2.5W at 15V, 3A load and 50% duty cycle (see Table 8.1.3.2). There was 45W passing through the converter with 2.5W loss. This gave 94.5% efficiency if MOSFET switching losses and capacitor ESR losses were negligible.

#### 8.1.4 Flyback Converter

The losses for the Flyback converter were also calculated for 3A and 15V.

Figure 6.3.3 shows the current waveform of a Flyback Converter. It was known that for a 3A load the Flyback experienced 12A current peaks (section 6.3). Equation 8.1.4.1 was used to find the RMS current at 50% duty cycle with 12A current peaks and gave 4.90A RMS.

Eq - 8.1.4.1 from Erickson A1.8 [19]
$I_{rms} = I_{pk} \sqrt{\frac{D}{3}}$

The MOSFET had a  $R_{on}$  of  $0.06\Omega$  and conducts 4.9A RMS during its on cycle. This gave 1440.6mW of power dissipated over each MOSFET, or 2881mW in total.

In addition to the MOSFET on losses there were; switching losses, core material flux losses, leakage inductance losses, and ESR losses. These were difficult to calculate.

Table 8.1.4.2 – Flyback Converter Losses

Component	Loss (mW)
Idle State Losses	385
MOSFET Gate Charge Losses	225
MOSFET On Resistance Losses	2881
MOSFET Switching Losses	?
Transformer Core Losses	?
Leakage Inductance Losses	?
Capacitor ESR Losses	?
Total	3491

The input into the Flyback was 15V and 3A, or 45W. Table 8.1.4.2 shows there was a loss of 3.5W, and hence the efficiency was 92%. However, the highest losses in the converter were expected to be the transformer core and leakage inductance losses. Consequently, the expected efficiency will be much lower than 92%.

## 8.2 Pspice Simulations

Appendix G contains the Pspice Circuits for an Isolated Cuk, a normal Cuk, and a Flyback converter. The extra resistances that were inserted in the circuits were to assist Pspice simulations from encountering infinite currents and voltages. These resistances also occurred in real hardware due to resistance in connectors and PCB tracks.

### 8.2.1 MOSFET Gate charge

A simple circuit was used to measure the power required to switch an IRFZ24N MOSFET. The IRFZ24N MOSFET had a gate charge of 20nC (Appendix B). Using the theoretical calculation method in section 8.1.2, the gate charge power dissipation should be 50mW at 5V. Pspice simulations gave 45mW for these conditions. For 15V the calculations gave 450mW to switch the gate. Pspice simulations gave 328mW.

This was a good correlation in theoretical calculations and simulation, and indicated that the calculations for the gate charge power dissipation were not significantly affected by the assumption that the gate fully charges.

### 8.2.2 Efficiency Comparison

The Cuk, Flyback, and Isolated Cuk were all simulated at 3A, 15V in and 15V out, to locate the losses they experienced.

Table 8.2.2.1 – Breakdown of Converter Losses

Cuk		Isolated Cuk		Flyback	
Name	Power (W)	Name	Power (W)	Name	Power (W)
In	46.893	In	47.550	In	51.100
Out	41.501	Out	41.265	Out	28.713
L3	0.357	L3	0.338	M4	1.201
L4	0.414	L4	0.501	M8	2.902
M6	1.284	M6	1.432	Resistors	18.284
M8	2.568	M7	1.092		
Resistors	0.768	Resistors	2.922		

Table 8.2.2.1 shows the various losses in the three converters. The component names match those found in the Pspice schematics found in Appendix G. From the power in and power out the efficiencies were determined to be 88.50%, 86.78%, and 56.19% for the Cuk, Isolated Cuk, and Flyback respectively. These efficiencies do not take into account ESR of capacitors, driving circuitry, sensing circuitry, transformer leakage inductance, or transformer core losses. Furthermore, in these simulations synchronous rectification was not used so the 2<sup>nd</sup> MOSFET losses are higher than what would be expected.

As stated earlier the power losses in the resistors were necessary to prevent simulation errors. These losses contributed significantly to the losses of the converters. The simulation was still valid as long as the resistor losses did not constitute the majority of the overall loss in the simulation.

For the Cuk converter the inductor losses L3 and L4 give a combined amount of 0.771W. This correlates to the theoretical calculated value of 0.763W. The MOSFETs had a greater loss than the 1.1W, which was calculated. The component M6 dissipates power through on resistance losses and switching losses. From calculations the on resistance losses for the Cuk was 0.545W. Subtracting this from the 1.284W dissipated through the MOSFET

M6, the expected switching losses were 0.739W. The MOSFET M8 was not being synchronously switched, instead functioning as a diode rectifier. Consequently, the power dissipation on M8 was significantly higher than M6.

The Isolated Cuk converter had similar properties as the Cuk converter. To prevent simulation errors larger resistors were used in this Pspice design. These resistors work as snubbers and reduced switching losses. This can be seen in the reduced power consumption of the MOSFETs. However, the resistors inserted their own losses, reducing the efficiency overall.

The Flyback converter does not reflect the actual characteristics of the real converter. The main problem encountered was the inability to simulate an air gap in the transformer. Without the air gap the transformer does not work as an energy storage device.

While efficiency results were not valid, the Pspice model was helpful in determining that the basic layout of the Flyback worked, as there was still partial functionality of the Flyback without the air gap. The main problem with the model was extremely high voltages and currents from direct transfer of energy to the secondary, whereas an air gap stored this energy before transferring. These required large resistances to allow simulation to occur and the effects of these resistances could be seen in the large resistive losses for the simulation results in Figure 8.2.2.1.

### 8.2.3 Load Variation

All three converters were simulated under various loads to measure their performance. The raw data obtained from these simulations can be found in Appendix H. The Flyback was not discussed, as it did not reflect the characteristics of the actual converter.

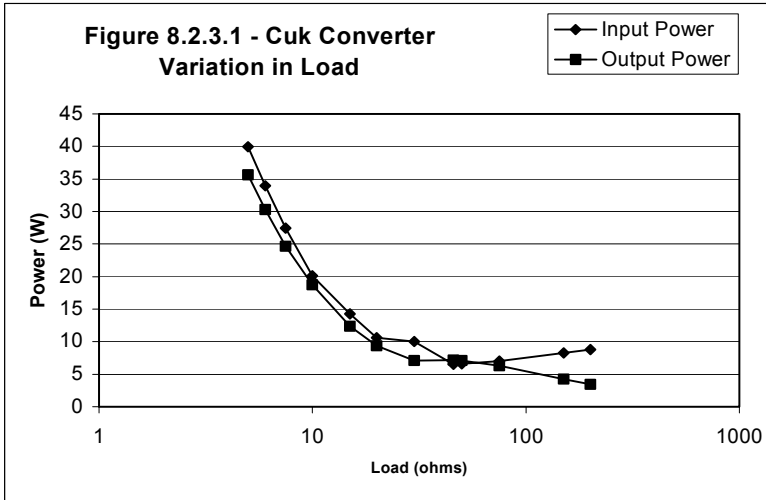


Figure 8.2.3.1 shows the various loads and their respective power consumption for the Cuk Converter.

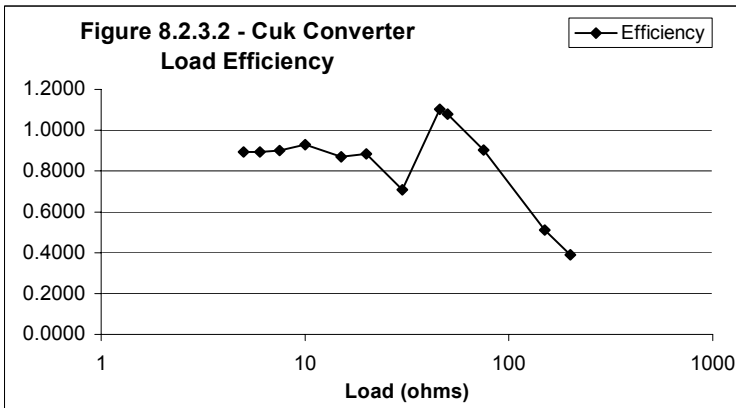


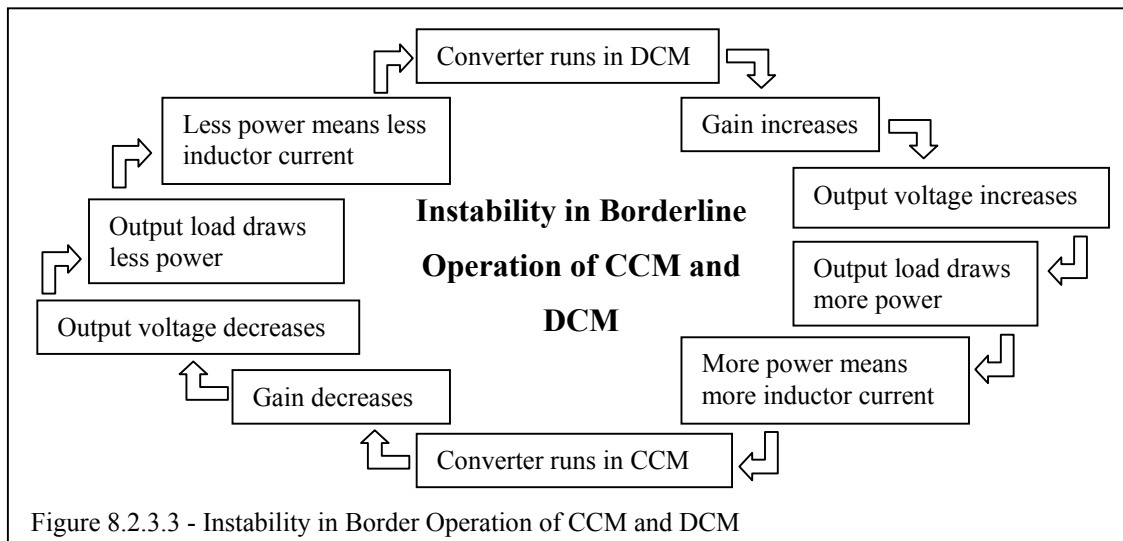
Figure 8.2.3.2 shows the efficiency of the converter under different loads. Around  $30\Omega$  to  $45\Omega$  for the load there was a sudden increase in the efficiency. The graph in Figure 8.2.3.2 showed efficiency above 100%. The cause of efficiency rise was from instability in the input and output currents. This caused measurement errors that required lengthy simulation periods to average the current over and remove.

While the three data points between loads 30 and 100 were inconsistent and were ignored, the cause of the instability was still a matter of concern.

From section 7.1, it was known that the Cuk converter operates in CCM in high loads and DCM in lower loads. Calculations for the 100uH inductor using equation 7.1.1 (with  $V_L = 15$  and a frequency of 100kHz) revealed there was a minimum  $\Delta i$  of 0.75A for the converter to remain in CCM. This translated into a minimum load of 0.35A average since the inductor waveform was a triangle wave. A 0.35A current load was equivalent to a 42.9Ω load at 15V out (using Ohms law).

At output loads around 42.9Ω the converter started switching between CCM and DCM. This was what generated the instability as CCM and DCM had different gains. Appendix H, Table H.1 shows that after 45.7Ω the output voltage of the converter started increasing as a duty cycle of 50% in the simulation no longer gave a unity gain.

Figure 8.2.3.3 shows how the Cuk converter will switch between CCM and DCM causing instability when the Cuk was operating at the borderline of CCM and DCM.



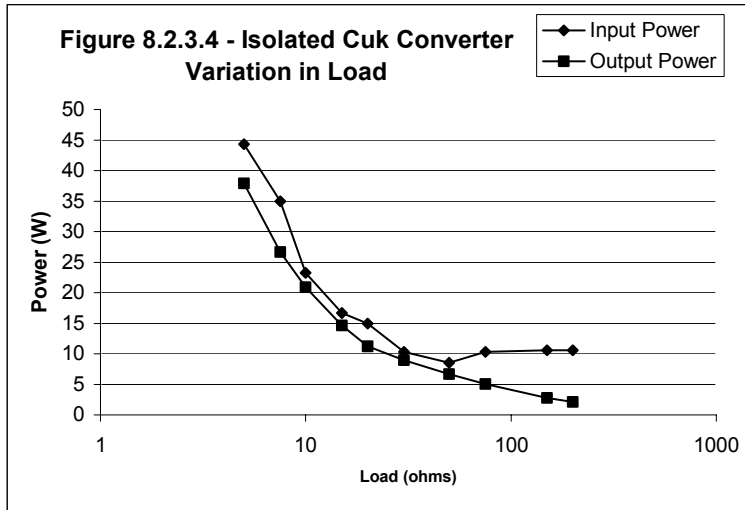
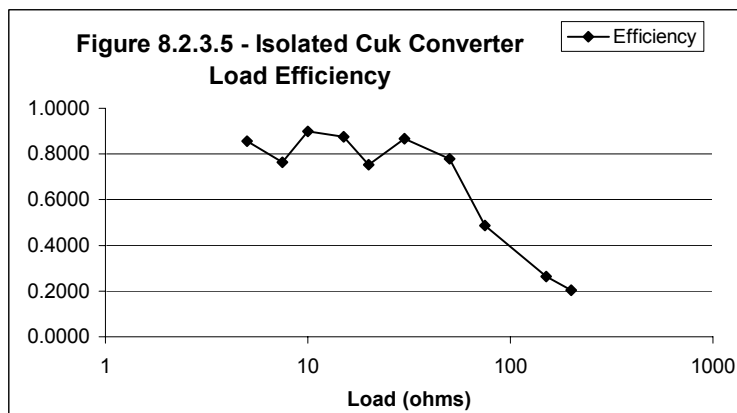


Figure 8.2.3.4 shows the various loads and their respective power consumption for the Isolated Cuk Converter.



As the Isolated Cuk converter uses the same inductor size as the Cuk, it began operating in DCM around the same load of 42.9Ω. It can be seen that for the Isolated Cuk topology there was significant decrease in efficiency when the converter switches to DCM. This has been made very obvious in the Isolated Cuk converter, as there were significantly more parasitic resistances placed in the circuit to allow for simulations. DCM operation generates higher currents and increases the affects of parasitic. This was described in section 6.4.

## 8.2.4 Synchronous Rectification

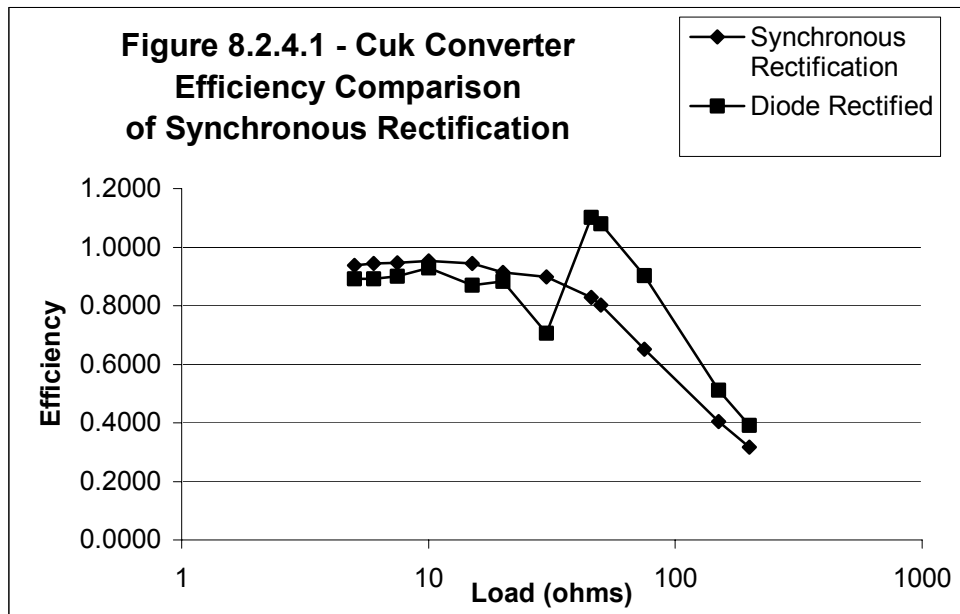


Figure 8.2.4.1 shows the efficiency comparison between a Cuk converter that was synchronously switched and one that was not. Synchronous Rectification, section 6.3, explained the advantages and disadvantages of synchronous rectification. These affects can now be seen in Figure 8.2.4.1.

As explained in section 8.2.3 a Cuk converter that was not synchronously switched enters into DCM, which caused instability in the gain of the converter. The synchronous Cuk did not experience DCM, and made a smooth transition through the loads that caused instability in the other Cuk.

When the lighter loads were reached the synchronous Cuk had a lower efficiency than the diode rectified Cuk. This was because the synchronous Cuk still had a 0.35A ripple current (calculated in section 8.2.3) to remain in CCM, while the diode rectified Cuk had a much smaller current running internally.

### 8.2.5 Frequency Variation

The design section made an educated guess at a suitable operational frequency for the converters. A full analysis of the frequency range in Pspice would be an extremely time consuming as each data point must be simulated. The chosen frequency was 100kHz. So the circuits were simulated at 50kHz and 200kHz to simply see if 100kHz was a reasonable choice.

Table 8.2.5.1 – Frequency Choice Confirmation

Frequency (kHz)	Cuk ( $\eta$ )	Synchronous Switched Cuk ( $\eta$ )	Isolated Cuk ( $\eta$ )	Flyback ( $\eta$ )
50	0.8862	0.9328	0.8550	0.5602
100	0.8924	0.9371	0.8553	0.5636
200	0.8877	0.9056	0.8449	0.5812

The results shown in Table 8.2.5.1 shows there were no significant efficiency gains that could be obtained by changing the frequency. All tests, excluding the Flyback, showed 100kHz to have a higher efficiency. As the Pspice Flyback model did not take into account many of the transformer affects, its results were unreliable. For the Cuk converters the Pspice suggested that 100kHz was a suitable frequency to run the converters at.

### 8.2.5 Pulse Transformer

The pulse transformer shown in Figure 6.6.4 was constructed in Pspice and tested. It was able to successfully reinsert the DC bias back into the gate drive signal with 1V offset. Analysis of the circuit revealed the 1N4001 diodes set the level of the DC bias. Appendix C shows that the 1N4001 has a forward voltage of 1V. The solution to this problem was to insert a schottky diode, the 1N5817, into the circuit. When the pulse transformer was re-simulated the offset of the signal through the circuit was 0.4V.

### 8.3 Breadboard Testing

The pulse transformer, which was described in section 6.6, was tested on the breadboard. 24 windings were made on both primary and secondary side of a toroid transformer. A 15V square wave signal was placed at the input and the output waveform was viewed on the oscilloscope. The input and output waveforms matched almost perfectly.

The pulse transformer was then tested with one of the converters. Only the Cuk converter was built on breadboard, as calculations for the Flyback transformer delayed its development for several weeks. The Cuk converter was switched on a single side using the pulse transformer and a function generator.

Table 8.3.1 – Cuk Isolated gate driver switching

Test Performed	$V_{in}$ (V)	$I_{in}$ (A)	$V_{out}$ (V)	Load ( $\Omega$ )	Efficiency ( $\eta$ )
no driver chip, isolated side	12.2	0.48	15	47	84%
driver chip, isolated side	15.5	0.45	16.8	47	89%

The tests performed in Table 8.3.1 were to confirm two important aspects of the Cuk converter design. First and foremost, the tests confirmed that the design for the Cuk converter would work. Secondly it confirmed that the pulse transformer was able to drive the Cuk converter with and without a driver chip.

Table 8.3.1 shows that the driver chip was able to switch the MOSFET faster reducing switching losses. The oscilloscope had a  $50\Omega$  output impedance, whereas the driver chip the UC3709 (Texas Instruments [38]) supplied 2A current peaks, making it equivalent to having  $7.5\Omega$  output impedance.

Further testing was delayed for correct components and the PCB, as these played a significant part in the efficiency and power rating of the converter.

## 8.4 First Prototypes

The microcontroller, 5V regulator, voltage sensor were all tested and worked.

The differential amplifier was tested for linearity.

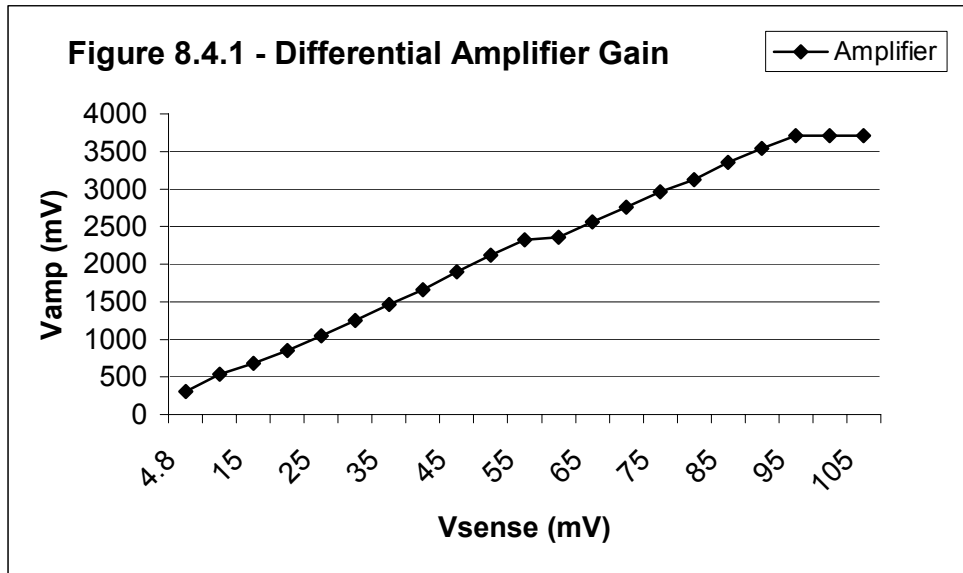


Figure 8.4.1 shows the linearity of the amplifier (raw data from Appendix I). The amplifier had a gain of 40 with a high linearity of voltage sensing between 25mV to 90mV. This corresponds to 1A to 4.5A of current detected by the current sensor. A glitch was seen at 60mV, this was caused by adjustment of the oscilloscope scaling and had nothing to do with the amplifier.

The Cuk converter was switched on both sides to check for bi-directionality. One side was switched at 15V and the other MOSFET operated as a diode.

Table 8.4.2 – Cuk Converter efficiency results

Test Performed	$V_{in}$ (V)	$I_{in}$ (A)	$V_{out}$ (V)	Load ( $\Omega$ )	Efficiency ( $\eta$ )
Cuk, isolated side	15.4	0.47	17.8	45.7	95.8%
Cuk, non-isolated side	15.5	0.45	17.5	45.7	96.1%

Table 8.4.2 shows the test results, with a 96% efficiency for both sides. However, due to limitations in the equipment accuracy the efficiency may vary. Assuming a 1% worst-case equipment error, the efficiency variation was 4%.

The next test to be performed was synchronous switching. The Atmel with the synchronous switching code, detailed in section 7.7, was inserted into the converter and both MOSFETs were destroyed. This test was repeated with similar results.

Analysis of the 4 destroyed MOSFETs revealed they functioned as resistors. The MOSFETs were not warm so overheating did not destroy them. The calculations for converter expected 30V drain source voltage and the IRFZ24N MOSFETs that were used had 55V drain source rating.

The MOSFET gate source rating was 16V and this was close to the 15V switching voltage. Measurement of the gate source resistance revealed the MOSFETs gate and source were now permanently connected. It was concluded that the MOSFET gates must have suffered voltage spikes when the power was turned on. This problem was not encountered in earlier testing as the gate switching waveform was always connected after the power supply had stabilized.

This problem prompted the redesign of the MOSFET driving to 5V, as explained in section 6.6.

The Flyback was tested with 7 turns and a 650 $\mu$ m effective air gap. This was calculated to give 200mT of flux at maximum load, and 200mT was the recommended operating flux for the core. This gave an efficiency of around 20%. The exact efficiency was not measured due to the characteristic burning smell of too much power being dissipated in the converter.

The air gap was removed and the transformer was rewound to 10 turns. This configuration was what was being used in Pspice simulations. Without an air gap the converter was still

able to work at light loads. However, theory suggested that the transformer saturated easily without an air gap. The Flyback converter was tested without an air gap to ensure the circuitry was correct even though the transformer was incorrect.

Table 8.4.2 – Flyback with un-gapped transformer

$V_{in}$ (V)	$I_{in}$ (A)	$V_{out}$ (V)	Load ( $\Omega$ )	Efficiency ( $\eta$ )
15.0	0.42	15.3	45.7	81.3%

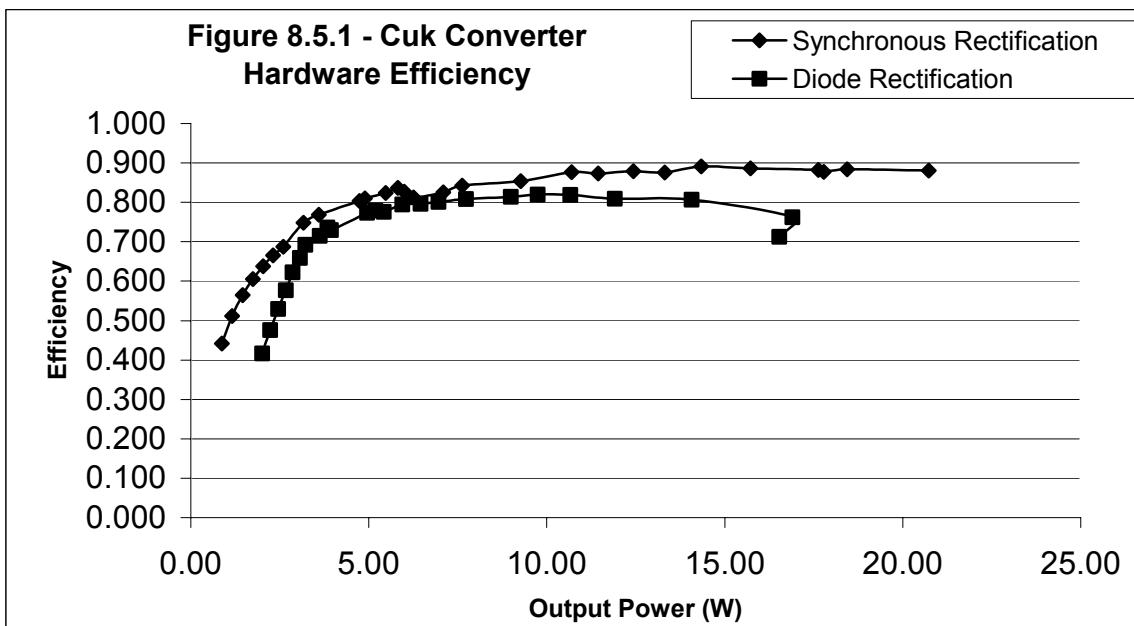
The success of this test, shown in Table 8.4.2, confirmed that the transformer was causing the problems with the Flyback, and the solution to the problem could be found by reanalysing the formulas.

## 8.5 Second Prototypes

The second prototypes of the Cuk and Flyback are detailed in implementation (section 7). These prototypes were confirmed to fit in the junction boxes of the PV modules.

The raw data from graphed efficiency testing can be found in Appendix J.

The Cuk converter was tested first and found to have no input and output ripple. The Cuk converter efficiency was characterized for both diode rectification and synchronous rectification starting from about 0.1A to 1.5A. Due to equipment failure of the ammeters, loads greater than 1.5A were not measured. This can be seen in Figure 8.5.1.



The Cuk converter was tested at 3A. The load on the output of the converter was reduced until 3.1A was being draw from the power supply at 14.7V. The output was measured to be 11.26V, and the load was then found to be 3.6Ω. This gave 3.1A at the output and hence the converter operated at 77% efficiency. The equipment that measured the load resistance was inaccurate at low resistances so the efficiency of 77% is not a real efficiency. It only showed that the Cuk converter still had reasonable efficiency at a 3A load.

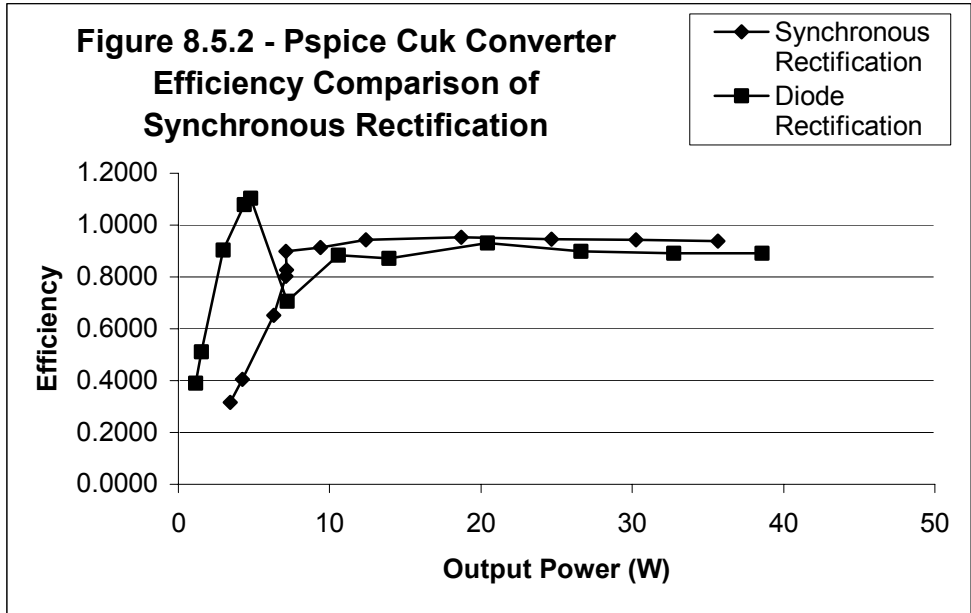


Figure 8.5.2 shows the expected efficiency characteristics from the Pspice simulations. The Pspice and hardware results were compared for discrepancies. Ignoring the glitch with the efficiencies above 100%, the only discrepancy was that the diode rectification for the Pspice had better efficiency at extremely low loads. This was due to unrealistically low resistances in the Pspice simulations.

Analysis of the raw data (Appendix J Table J.1) revealed that the diode rectification always drew 0.3A at all loads lighter than 0.3A. From the earlier analysis that determined the border load of DCM and CCM, it was known that 0.3A was the borderline between the two modes. Furthermore, the synchronous rectification did not experience this problem. Analysis revealed that when the converter entered DCM operation, the output voltage of the converter increased. The 1N5822 schottky diode in parallel to the MOSFET drain source had a RMS voltage rating of 28V. It was previously assumed with an output of 15V this voltage rating was not exceeded. However, test results indicated otherwise.

Pspice analysis of the Cuk converter at light loads revealed the schottky diode voltage rating was exceeded when the converter entered DCM and the output voltage increased due to the increased gain of the converter. This caused the high losses for the Cuk converter when it operated in DCM, as the schottky was experiencing reverse breakdown due to the higher voltages.

The schottky diode was removed from the converter and a comparison was done for both diode rectification and synchronous.

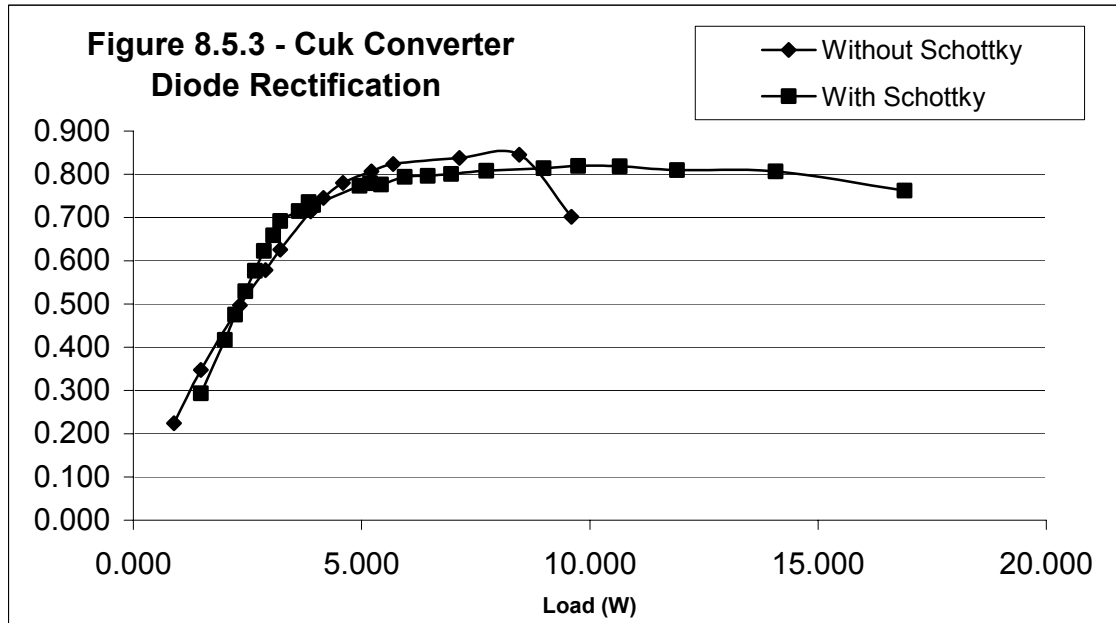


Figure 8.5.3 shows that the diode rectified Cuk Converter was slightly more efficient at very light load when the schottky was removed. However, without the schottky diode there were increased MOSFET losses as the MOSFET was being used as a diode, and forward voltage drop of the MOSFET was higher than the forward voltage drop for the schottky.

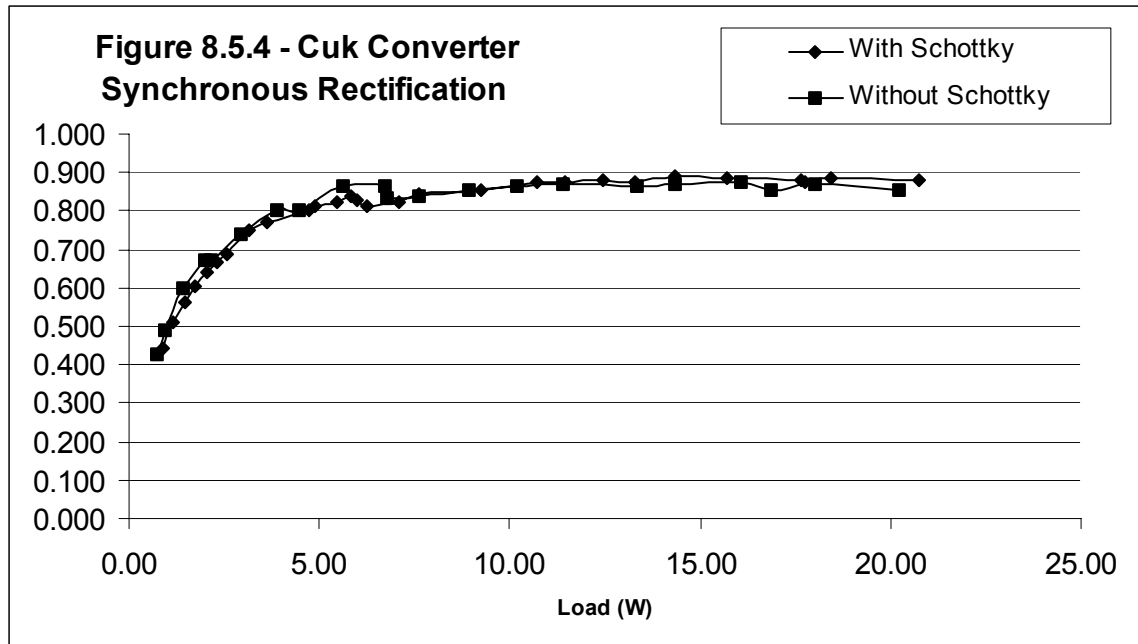
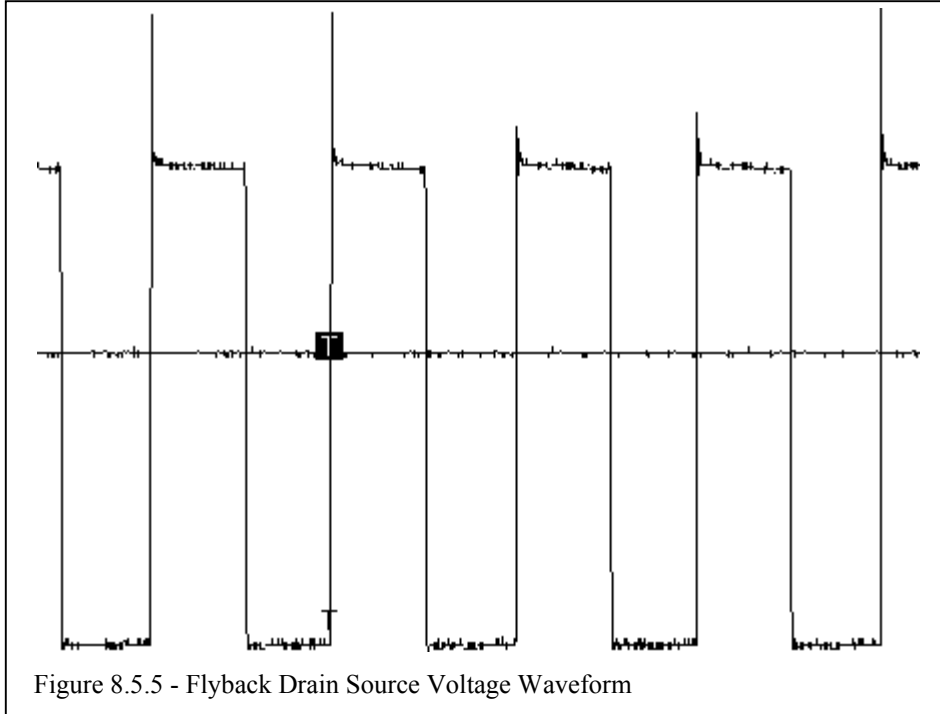


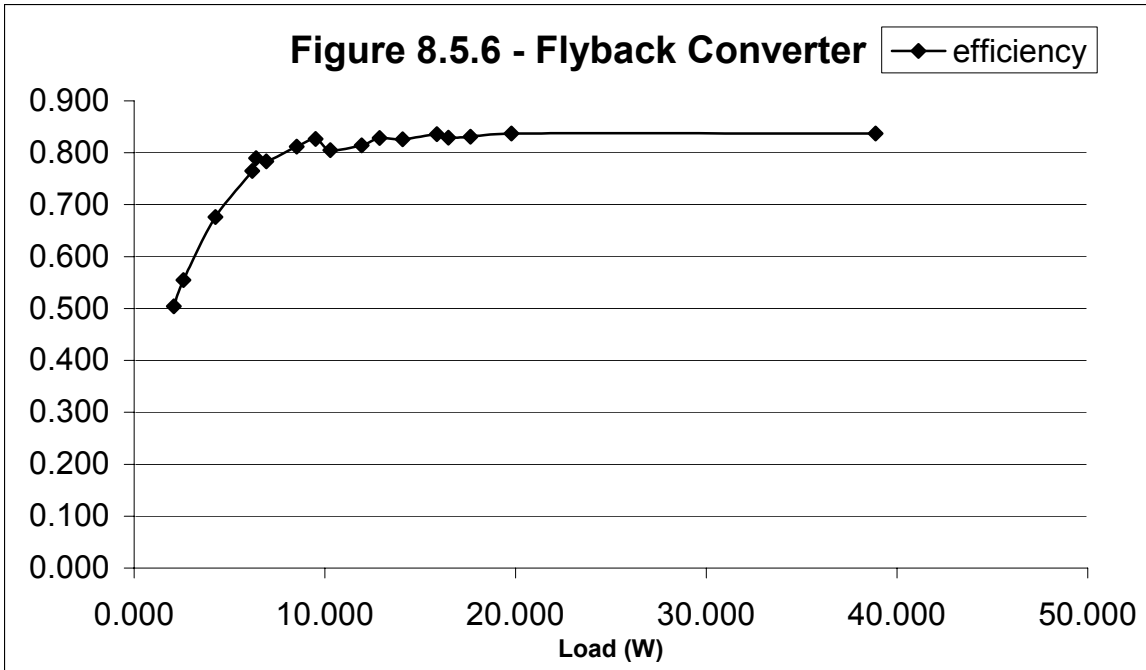
Figure 8.5.4 shows the synchronous rectified Cuk converter. There was very little difference in the converter operation when the schottky diode parallel to the MOSFET was removed.

From the data, the second Cuk prototype had an efficiency of 82% at 6.6W load compared to 96% for the first prototype at the same load. This was because the MOSFETs were originally switched at 15V. In the second prototype the MOSFETs were switched at 5V and there were increased switching losses as 5V switched the MOSFETs slower.

The Flyback converter was tested next. A 0.2mm effective air gap was inserted into the Flyback and 7 turns were wound for the primary and secondary. Minimal input and output ripple was observed, well within the designed for tolerance.



The drain source voltage of both MOSFETs were measured to determine the over voltage caused by the transformer leakage inductance. This is shown in Figure 8.5.5. The leakage inductance appeared to be minimal for the transformer so the snubber described in Figure 6.3.6 was not implemented.



The Flyback converter was tested under various loads. Figure 8.5.6 showed the results of these tests. Overall the Flyback Converter performs slightly worse than the Cuk converter. This is mainly due to losses in the transformer, such as the skin effect.

## **9.0 Closure**

### **9.1 Future Work**

The software for the MPPT tracking needs to be adjusted so it no longer requires interrupts. This can be started as soon as the ATmega8535 chips are available.

The software tracking algorithm can be improved from the Perturb and Observe algorithm to the Slope Tracking algorithm detailed in the Design section of this thesis.

Hardware testing has also revealed that a low voltage protector will improve the initial start up of the converter and protect the converter when the solar panels are not generating enough voltage to run the converters.

Finally the system needs to be installed on a set of solar cells and the effectiveness of the system should be evaluated.

Additional tasks that may be considered are; implementation of a network to allow for panel monitoring during tests, microcontroller code to turn off the converters when the panel does not require maximum power point tracking, and Pspice or hardware testing to determine the optimal frequency to switch the converters at.

## **9.2 Evaluation of Performance**

This thesis was mainly chosen as a means to balance technical knowledge of digital systems and software with some applied knowledge of analogue electronics. Consequently, the main weakness during the course of this thesis was the lack of understanding and experience in the field of power electronics.

One of the most important lessons learnt was obtaining feedback from the supervisor and discussion of problems with other students working on similar design problems. This dramatically increases the progress of the work. In the first few months of the thesis large amounts of time were spent working alone with minimal dialogue with the supervisor and other students. Consequently, the work in the early stages progressed very slowly, especially as much of the theory was learnt directly from textbooks and papers, which are often difficult to understand. Progress was increased several fold when problems were discussed with the supervisor and other students.

The original objective of the thesis was to complete all the basic hardware with simple MPPT tracking of the PV modules. The difficulties of doing this were severely underestimated and consequently the thesis was completed two weeks later than expected.

This thesis has made significant progress the research and design of PV module series string balancing converters. In addition to the actual progress of the design, a vast number of the problems, ideas and theory that were encountered have been recorded in this thesis document. Learning and understanding all the theory has slowed the progress of the actual thesis. However, understanding theory allows for many problems to be avoided. This paves the way for future students, and will significantly improve the quality, and development time of future work. The theory and problems explored in this thesis are relevant to any thesis involving power electronics and this thesis can be a useful guide to various power electronics issues.

### **9.3 Conclusion**

The final goal of evaluating the theory of PV module series string balancing converters is well on the path to completion. Significant progress has been made in the realisation of module balancing converters with hardware finalised. While the original goals of the project were not met, it was decided these are unrealistic due to the large quantity of work required.

The hardware is almost complete with minor adjustments required for the Flyback transformer to accommodate higher loads. The circuitry for the MPPT and switching have been tested and work. The Cuk Converter works with efficiencies greater than 80% for the majority of its load range, and efficiencies greater than 85% for all measured loads above 0.7A. The Flyback converter has been proven to work for the required power range with efficiency greater than 80% for all loads above 0.6A. The hardware fits in the junction boxes of the PV modules. A simple MPPT algorithm has implemented and a more complex algorithm for tracking has been designed though not implemented.

Furthermore, extensive documentation and explanations into the theory related to the thesis have been compiled in this document. This thesis provides a firm foundation for future work, and provides a reference on many power electronics issues for future students.

## 10.0 References

- [1] - World Resources Institute (July 25 2001), "Climate news from Bonn"  
[http://www.wri.org/jlash/climate\\_news.html](http://www.wri.org/jlash/climate_news.html), retrieved on 25/4/02
- [2] - The Sustainable Development Fund (Dec 2001), SDF's Solar PV Grant Program  
<http://www.trfund.com/sdf/solarpv/index.html>, retrieved on 22/3/02
- [3] - New Engery (2001), Subsidy Program for Residential PV systems.  
<http://www.nef.or.jp/english/moniter/moni1.htm>, retrieved on 22/3/02
- [4] - Solarbuzz (2001), Uses of Solar Energy  
<http://www.solarbuzz.com/Applications.htm>, retrieved on 22/3/02
- [5] - Paul Maycock(Jan 1999), US PV NEWS EXCERPT  
<http://www.pvenergy.com/article.html>, retrieved on 22/3/02
- [6] - Björn Lindgren (2000), A Power Converter for Photovoltaic Applications  
[http://www.elkraft.chalmers.se/Publikationer/EMKE.publ/Abstracts/LindgrenLic\\_00.pdf](http://www.elkraft.chalmers.se/Publikationer/EMKE.publ/Abstracts/LindgrenLic_00.pdf),  
retrieved on 1/4/02
- [7] - NoOutage.com uc (20/08/01), 101W 120VAC Solar PV Module  
[www.nooutage.com/es112.htm](http://www.nooutage.com/es112.htm), retrieved on 22/3/02
- [8] - Ascension Technology, Inc. (1998), SunSine™300 AC Photovoltaic Module  
Installation, Operation and Maintenance Manual.  
<http://www.appliedpower.com/PDF/ATISSManual.pdf>, retrieved on 1/4/02
- [9] - ABC radio, "Advances bring closer the promise of solar power",  
<http://www.abc.net.au/worldtoday/s49182.htm>, retrieved on 10/10/02
- [10] - Björn Lindgren (2000), A PV-module Oriented Inverter, Feeding a Low Voltage  
AC Bus,  
<http://www.elkraft.chalmers.se/Publikationer/EMKE.publ/Abstracts/euroPV00.pdf>,  
retrieved on 1/4/02
- [11] - Konrad Mauch (2001). Progress in Inverter Technology for PV Systems  
<http://www.sandia.gov/pv/symposium/B3 - Mauch.doc>, retrieved on 1/4/02
- [12] - J. Riatsch, H. Stemmler and R. Schmidt, "Single Cell Module Integrated Converter  
System for Photovoltaic Energy Generation", Proceedings of the 7<sup>th</sup> European Conference  
on Power Electronics and Applications, Trondheim 1997.
- [13] - Toshihisa shimizu. "Generation Control Circuit for Photovoltaic Modules". IEEE  
Transactions on power electronics, VOL 16 No 3, May 2001, p293-300
- [13.5] - Toshihisa shimizu (2001), Generation Control Circuit for Photovoltaic Modules  
(In Japanese). [http://www.furukawadenchi.co.jp/tech/pdf/fbtn56\\_106.pdf](http://www.furukawadenchi.co.jp/tech/pdf/fbtn56_106.pdf), retrieved on  
1/4/02
- [14] - C. Hua and C. Shen, "Study of maximum Power Point Tracking Techniques and  
Control of DC/DC Converters for Photovoltaic Power Systems", IEEE 29nd Annual  
Power Electronics Specialists Conference, p.86-93, 1998.
- [15] - Moraes R, "Description and Modeling of the Individual Components of a  
Photovoltaic Pumping System", [http://docserver.bis.uni-  
oldenburg.de/publikationen/dissertation/2000/morana00/pdf/kap03.pdf](http://docserver.bis.uni-oldenburg.de/publikationen/dissertation/2000/morana00/pdf/kap03.pdf), retrieved on  
10/10/02
- [16] - Toshihiko Noguchi, Shigenori Togashi, Ryo Nakamoto, "Short-Current Pulse-  
Based Maximum-Power-Point Tracking Method for Multiple Photovoltaic-and-Converter  
Module System", IEEE Transactions on Industrial Electronics. vol. 49, p.217-223, 2002

- [17] - K. K. Tse, Henry S. H. Chung, S. Y. R. Hui, and M. T. Ho, "A Novel Maximum Power point Tracking Technique for PV Panels", IEEE 32nd Annual Power Electronics Specialists Conference, vol. 4, p.1970-1975, 2001.
- [18] - Shengyi Liu (09/05/00), "Maximum Power Point Tracker Model", [http://vtb.engr.sc.edu/modellibrary\\_old/pdf/controller\\_mppt.pdf](http://vtb.engr.sc.edu/modellibrary_old/pdf/controller_mppt.pdf), retrieved on 3/10/02
- [19] - Robert W. Erickson, "Fundamentals of Power electronics", Kluwer Academic Publishers, USA, 1997.
- [20] - Steve Watkins (1998), "HISTORY AND DEVELOPMENT OF SWITCHED-MODE POWER SUPPLIES PRE 1987" <http://www.steve-w.dircon.co.uk/fleadh/mphil/history.htm>, retrieved on 16/8/02
- [21] - Ferroxcube, [www.ferroxcube.com](http://www.ferroxcube.com), retrieved 22/8/02
- [22] - Paul A. Tipler, "Physics for scientists and engineers", 4<sup>th</sup> Ed, Worth Publishers Inc, New York, 1990.
- [23] - unknown author, "The flyback converter - lecture notes ECEN4517", [http://ece-www.colorado.edu/~ecen4517/course\\_material/Exp6/flyback.pdf](http://ece-www.colorado.edu/~ecen4517/course_material/Exp6/flyback.pdf), retrieved on 23/8/02
- [24] - Matthew Greaves (August 2002), explanation on transformer theory
- [25] - Steward Home, "Glossary", <http://www.bravoelectro.com/html/stetngls.html>, retrieved 01/10/02. (Note: Glossary of magnetic theory terms)
- [26] - Michele Sclocchi (Feb 2001), "Design of a flyback switching power supply with the LM3488 low-side N-channel current mode controller", [http://www.national.com/appinfo/power/files/flyback-LM3488rev\\_E.doc](http://www.national.com/appinfo/power/files/flyback-LM3488rev_E.doc), retrieved 26/8/02
- [27] - Maxim 01/31/01, "Synchronous Rectification Aids Low-Voltage Power Supplies" [http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/652](http://www.maxim-ic.com/appnotes.cfm/appnote_number/652), retrieved on 29/4/02
- [28] - Atmel (November 2001), "AT90S/LS8535" <http://www.atmel.com/atmel/acrobat/doc1041.pdf>, retrieved on 17/7/02
- [29] - Atmel (September 2002), "ATmega8535(L) Advance Information", <http://www.atmel.com/atmel/acrobat/doc2502.pdf>, retrieved on 22/9/02
- [30] - Fritz Schlunder (December 2001), "High Side MOSFET Gate Drive: The Power of Well Implemented Pulse Transformers" <http://dsms.ajud.org/~fritz/AN1.pdf>, retrieved on 18/8/02
- [31] - University of Utah (2002), "Concavity and the Second Derivative", [http://www.math.utah.edu/online/1210/notes/Concavity\\_And\\_Second\\_Deriv.html](http://www.math.utah.edu/online/1210/notes/Concavity_And_Second_Deriv.html), retrieved on 3/10/02
- [32] - Steven R. Shaw, "Differential op-amp analysis", <http://matrix.coe.montana.edu/sshaw/classes/class-problems/problemc/step6.php3>, retrieved on 4/10/02
- [33] - Farnell, [www.farnell.com/australia/](http://www.farnell.com/australia/)
- [34] - Mohan, Undeland and Robbins, "Power Electronics", 2<sup>nd</sup> ed, Hamilton Printing Company, Canada, 1995
- [35] - Ferroxcube, "ETD29", <http://www.ferroxcube.com/prod/assets/etd29.pdf>, retrieved 22/8/02
- [36] - Ferroxcube, "EFD25", <http://www.ferroxcube.com/prod/assets/efd25.pdf>, retrieved 22/8/02
- [37] - EPCOS (23/02/01), "N87 material with improved properties", <http://www.eastern-components.com/pdf/ECI-211.PDF>, retrieved 21/9/02

- [38] - Texas Instruments (November 1997), "TPS2811, TPS2812, TPS2813, TPS2814, TPS2815 DUAL HIGH-SPEED MOSFET DRIVERS", <http://www-s.ti.com/sc/ds/tps2812.pdf>, retrieved on 19/8/02
- [39] - AVR GCC, <http://www.avrfreaks.net/AVRGCC/index.php>, retrieved on 30/7/02
- [40] - Sunlight Solar Australia Limited (September 2001), Solar Panel Pricing Table [http://www.sunlightsolar.com.au/solar\\_panels.html](http://www.sunlightsolar.com.au/solar_panels.html), retrieved on 7/4/02
- [41] - Geoffrey Walker (29/08/02), "Index of /~elec4400/datashts", <http://www.itee.uq.edu.au/~elec4400/datashts/>, retrieved 21/7/02
- [42] - Harald Kipp (22/8/02), "GCC AVR Inline Assembler Codebook Version 1.6", <http://www.egnite.de/ethernut/GCCAVRInlAsmCB.pdf>, retrieved on 19/9/02

## 11.0 Bibliography

- [43] - Thanh Phu Nguyen (2001), Solar Panel Maximum Power Point Tracker <http://innovexpo.itee.uq.edu.au/projects/s369584/thesis.pdf>, retrieved on 14/3/02
- [44] - Simon Kuan-Yu Su (2000), Solar Peak Power Point Tracker <http://innovexpo.itee.uq.edu.au/2000/348795970.htm>, retrieved on 14/3/02
- [45] - Sandia National Laboratroies (22/4/97), Photovoltaic Modules <http://www.sandia.gov/pv/comp/PVmodules.html>, retrieved on 22/3/02
- [46] - Klaus Bücher, Markus Danner, Andreas Kresse, Hermann Laukamp (5/5/99), The Influence of Extreme Operating Conditions on PV Modules <http://www.ise.fhg.de/Projects/components99/art1.html>, retrieved on 22/3/02
- [47] - Korupp k. h. (23/02/1998), IMPACT PROJECT FOR A NEW GENERATION OF PV GRID CONNECTED SYSTEMS (GP CAMPAIGN CYRUS) WITH ADVANCED TECHNOLOGIES AND MARKET, <http://europa.eu.int/comm/energy/library/se97.pdf>, retrieved on 22/3/02
- [48] - CIEMAT (february 2000), Improvement of Photovoltaic Modules - Measures for withstanding electrical and thermal effects caused by reverse biasing of cells (Project acronym: IMOTHEE), <http://www.ciemat.es/sweb/p480/imothee/abstract.pdf>, retrieved on 22/3/02
- [49] - Christian Schweizer (2000), Modelling Photovoltaic Systems in Urban Environments, [http://www.iesd.dmu.ac.uk/research\\_degrees/projects/schweizer.htm](http://www.iesd.dmu.ac.uk/research_degrees/projects/schweizer.htm), retrieved on 22/3/02
- [50] - pvpower.com (24 Feb 97), PV TECHNOLOGIES <http://www.pvpower.com/pvtechs.html>, retrieved on 23/3/02
- [51] - Sandia (2000), PV reliability database. <http://www.sandia.gov/pv/reliability.htm>, retrieved on 1/4/02
- [52] - Russell Bonn, Greg Kern, Jerry Ginn, Sigifredo Gonzalez (January 26, 1999), Standardized Anti-Islanding Test Plan, <http://www.sandia.gov/pv/bos/antiisland.pdf>, retrieved on 1/4/02
- [53] - Nasser H. Kutkut, Deepakraj M. Divean, Donald W. Novontny, "Charge equalization for series connected battery strings.", IEEE Transactions on Industry Applications, Vol. 31, p.562-568, May/June 1995.
- [54] - M. Veerachary, T. Senjyu and K. Uezato, "Maximum power point tracking control of IDB converter supplied PV system", IEE Proceedings Electric Power Applications, vol. 148, no.6, p. 494-502, 2001.

[55] - Osamu Hashimoto, Toshihisa Shimizu, Gunji Kimura, "A Novel High Performance Utility Interactive Photovoltaic Inverter System", Conference record of the 2000 IEEE Industry Applications Conference, vol 4, p.2255-2260, 2000.

[56] - Hisao Watanabe, Toshihisa Shimizu, Gunji Kimura, "A Novel Utility Interactive Photovoltaic Inverter with Generation Control Circuit", IECON '98. Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society, vol. 2, p.721-725, 1998.

[57] - unknown author, no title, <http://scholar.lib.vt.edu/theses/available/etd-4198-143730/unrestricted/Ch1.pdf>, retrieved 20/8/02 (Note: research into improving isolated converter designs)

[58] - unknown author, "Lecture 14, Disadvantages of Transformers and Introduction to the Flyback Converter",  
<http://www.engr.colostate.edu/ece/pages/courses/collins/ee562fall01/98lect~1/114.pdf>,  
retrieved on 22/8/02

[59] - Maxim (31/01/02), "Regulator Topologies For Battery-Powered Systems",  
[http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/660](http://www.maxim-ic.com/appnotes.cfm/appnote_number/660), retrieved 6/10/02

# Appendix A - Panel Specifications

Data obtained from sunlight solar [40] on 7/4/02.

	Panel	Power	RRPex	Nominal	Peak	Self	Peak	L x W x H	Weight	\$s per	Warranty
	Model	Watts	\$	Voltage	Voltage	Regulating	Current	mm	Kg	Watt	Years
Manufacturer											
	BP1202	2	\$96.00	12	17	NO	0.12	275 x 145 x 17	0.4	\$48.00	20
	BP1205	5	\$126.00	12	17	NO	0.29	275 x 231 x 17	0.8	\$25.20	20
	BP212SR	12	\$262.00	12	15.2	YES	0.72	561 x 231 x 38.5	1.6	\$21.80	20
	BP216SR	16	\$307.00	12	15.2	YES	1.07	558 x 277 x 43.5	2.8	\$19.10	20
	BP222SR	22	\$360.00	12	15.2	YES	1.45	443 x 530 x 43.5	2.8	\$16.30	20
	BP232SR	32	\$450.00	12	15.2	YES	2.13	627 x 530 x 43.5	5	\$14.00	20
	BP246SR	46	\$555.00	12	15.2	YES	3	825 x 530 x 43.5	5.5	\$12.10	20
	BP240	40	\$481.00	12	17	NO	2.34	627 x 530 x 43.5	5	\$12.00	20
	BP250	50	\$598.00	12	17	NO	2.94	825 x 530 x 43.5	5.5	\$11.90	20
	BP275	75	\$747.00	12	17	NO	4.45	1188 x 530 x 43.5	7.2	\$10.00	20
Kyocera	KC 35	35	\$354.00	12	15	NO	2.33	471 x 652 x 52	4.8	\$10.10	25
	KC 40	40	\$402.00	12	16.9	NO	2.34	526 x 652 x 52	6	\$10.10	25
	KC 60	60	\$528.00	12	16.9	NO	3.55	751 x 652 x 52	7.8	\$8.80	25
	KC 80	80	\$702.00	12	16.9	NO	4.73	976 x 652 x 52	9.6	\$8.80	25
	KC 120	120	\$1,056.00	12	16.9	NO	7.1	1425 x 652 x 52	11.9	\$8.80	25
UniSolar	US 64	64	\$600.00	12	16.5	NO	3.88	1366 x 741 x 32	9.17	\$9.40	20
Semi rigid panels ideal for use in transport applications or where rough handling is expected	US 42	42	\$447.60	12	16.5	NO	2.54	928 x 741 x 32	6.27	\$10.70	20
	US 32	32	\$372.00	12	16.5	NO	1.94	1366 x 383 x 32	4.8	\$11.60	20
	US 21	21	\$254.40	12	16.5	NO	1.27	928 x 383 x 32	2.99	\$12.10	20
	US 11	11	\$186.00	12	16.5	NO	0.62	491 x 383 x 22	1.63	\$16.90	20
	US 5	5	\$114.00	12	16.5	NO	0.3	491 x 205 x 22	1.13	\$22.80	20
Solarex Multimount	SX5M	4.5	\$140.00	12	16.5	NO	0.27	250 x 269 x 23	0.8	\$30.90	10
	SX10M	10	\$180.00	12	16.8	NO	0.59	421 x 269 x 23	1.5	\$18.00	10
	SX20M	20	\$285.00	12	16.8	NO	1.19	421 x 501 x 23	2.5	\$14.20	10
	SX30M	30	\$339.00	12	16.8	NO	1.78	593 x 501 x 23	3.5	\$11.30	10
	SX40M	40	\$414.00	12	16.8	NO	2.37	764 x 501 x 23	4.9	\$10.30	20
	SX50M	50	\$489.00	12	16.8	NO	2.97	938 x 501 x 23	5.7	\$9.80	20
Solarex Standard	MSX5L	4.5	\$185.00	12	16.8	NO	0.27	273 x 267 x 9	0.7	\$41.00	5
	MSX10L	10	\$246.00	12	17.1	NO	0.58	444 x 267 x 9	1.1	\$24.60	5
	MSX20L	20	\$383.00	12	17.1	NO	1.17	444 x 495 x 9	2.1	\$19.10	5
	MSX30L	30	\$484.00	12	17.1	NO	1.75	616 x 495 x 9	3	\$16.10	5
	MSX60	60	\$612.00	12	17.1	NO	3.5	1113 x 502 x 50	7.2	\$10.20	20
	MSX64	64	\$653.00	12	17.5	NO	3.66	1113 x 502 x 50	7.2	\$10.20	20
	MSX77	77	\$777.00	12	16.9	NO	4.56	1113 x 660 x 50	9.5	\$10.10	20
	MSX83	83	\$888.00	12	17.1	NO	4.85	1113 x 660 x 50	9.5	\$10.70	20
	MSX120	120	\$1,285.00	12	17.1	NO	7	1113 x 996 x 50	14.4	\$10.70	20
Solarex Universal	SX20U	20	\$289.00	12	16.8	NO	1.19	424 x 502 x 50	3	\$14.40	10
	SX30U	30	\$350.00	12	16.8	NO	1.78	594 x 502 x 50	3.9	\$11.60	10
	SX40U	40	\$419.00	12	16.8	NO	2.37	767 x 502 x 50	5.4	\$10.50	20
	SX50U	50	\$504.00	12	16.8	NO	2.97	939 x 502 x 50	6.3	\$10.10	20
	SX55U	55	\$534.00	12	16.5	NO	3.33	1110 x 502 x 50	7.2	\$9.70	20
	SX60U	60	\$594.00	12	16.8	NO	3.56	1110 x 502 x 50	7.2	\$9.90	20
	SX65U	65	\$639.00	12	17.2	NO	3.77	1110 x 502 x 50	7.2	\$9.80	20
	SX75U	75	\$745.00	12	16.5	NO	4.54	1461 x 502 x 50	9.5	\$9.90	20
	SX80U	80	\$772.00	12	16.8	NO	4.75	1461 x 502 x 50	9.5	\$9.60	20
	SX85U	85	\$825.00	12	17.1	NO	4.97	1461 x 502 x 50	9.5	\$9.70	20

## Appendix B – MOSFETs

TYPE	V <sub>DSS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	V <sub>GS(th)</sub> (V)	Q <sub>g</sub> (nC)	Q <sub>gs</sub> (nC)
BUZ11	50	0.040	33	2.1 – 4	?	?
IRF520	100	0.270	9.2	2 – 4	16	4.4
IRFZ24N	55	0.070	17	2 – 4	20	5.3
IRFZ34N	55	0.040	29	2 – 4	34	6.8
IRFZ44N	55	0.022	49	2 – 4	65	12
IRLZ24N	55	0.060	18	1 – 2	15	3.7
IRLZ34N	55	0.035	30	1 – 2	25	5.2
IRLZ44N	55	0.022	47	1 – 2	48	8.6
MTP3055E	55	0.150	14	2 – 4	15	7
RFD14N05	50	0.150	14	2 – 4	40	?
RFD15P05	50	0.100	15	-2 – -4	150	?
RFD3055	60	0.150	12	2 – 4	23	?
RFD3055LE	60	0.150	12	1 – 2	35	?

Information from [41]

## Appendix C – Diodes

Diode	Peak V (V)	Once peak (V)	RMS (V)	Surge I (A)	Average I (A)	Forward drop (V)
1N5817	20	24	14	25	1	0.32
1N4001	50	60	35	30	1	0.93
1N4002	100	120	70	30	1	0.93
1N5820	20	24	14	80	3	0.37
1N5821	30	36	21	80	3	0.38
1N5822	40	48	28	80	3	0.39
1N5400	50	100	35.4	200	3	1.2
MBR2035CT	35	?	?	150	20	0.57- 0.84
MBR2045CT	45	?	?	150	20	0.57- 0.84

Information from [41]

# Appendix D - Hardware Schematics

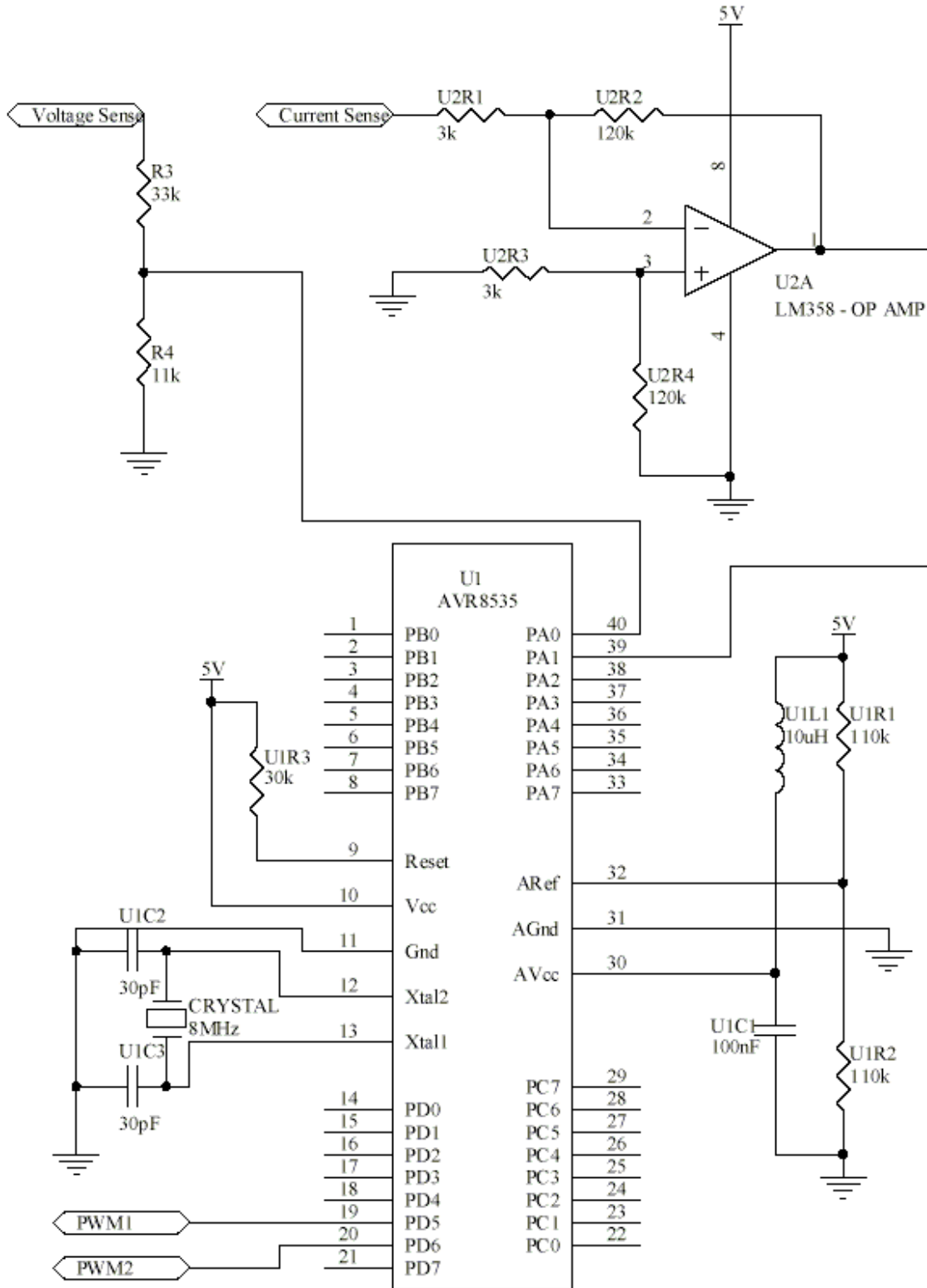


Figure D.1 - AT90S8535 and sensing circuitry

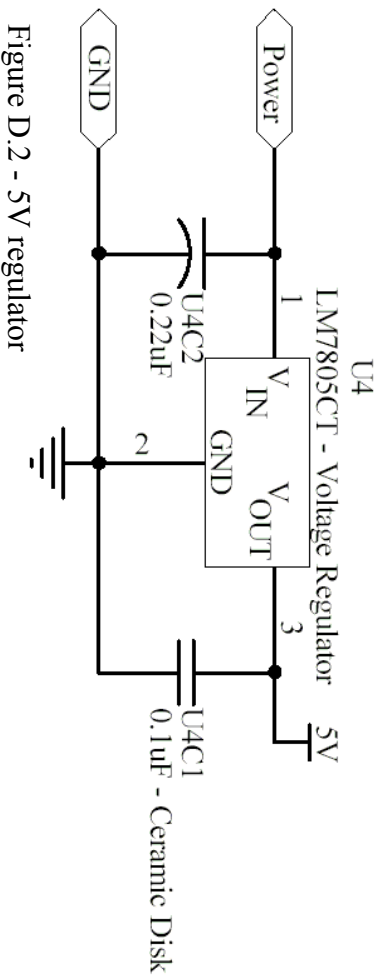


Figure D.2 - 5V regulator

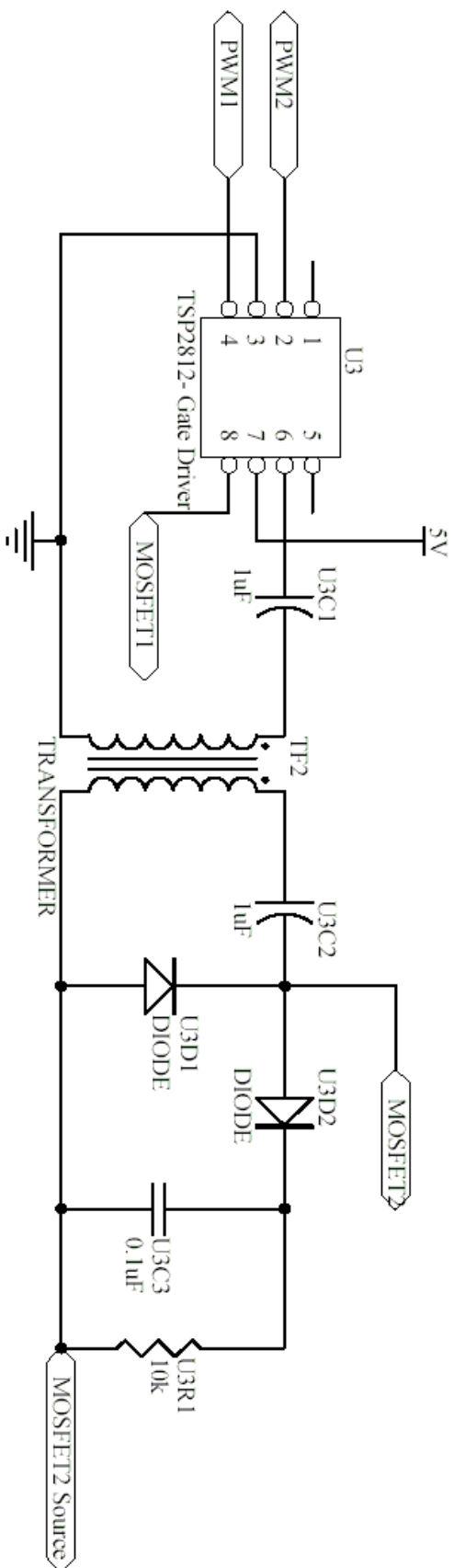


Figure D.3 - Driver Circuitry

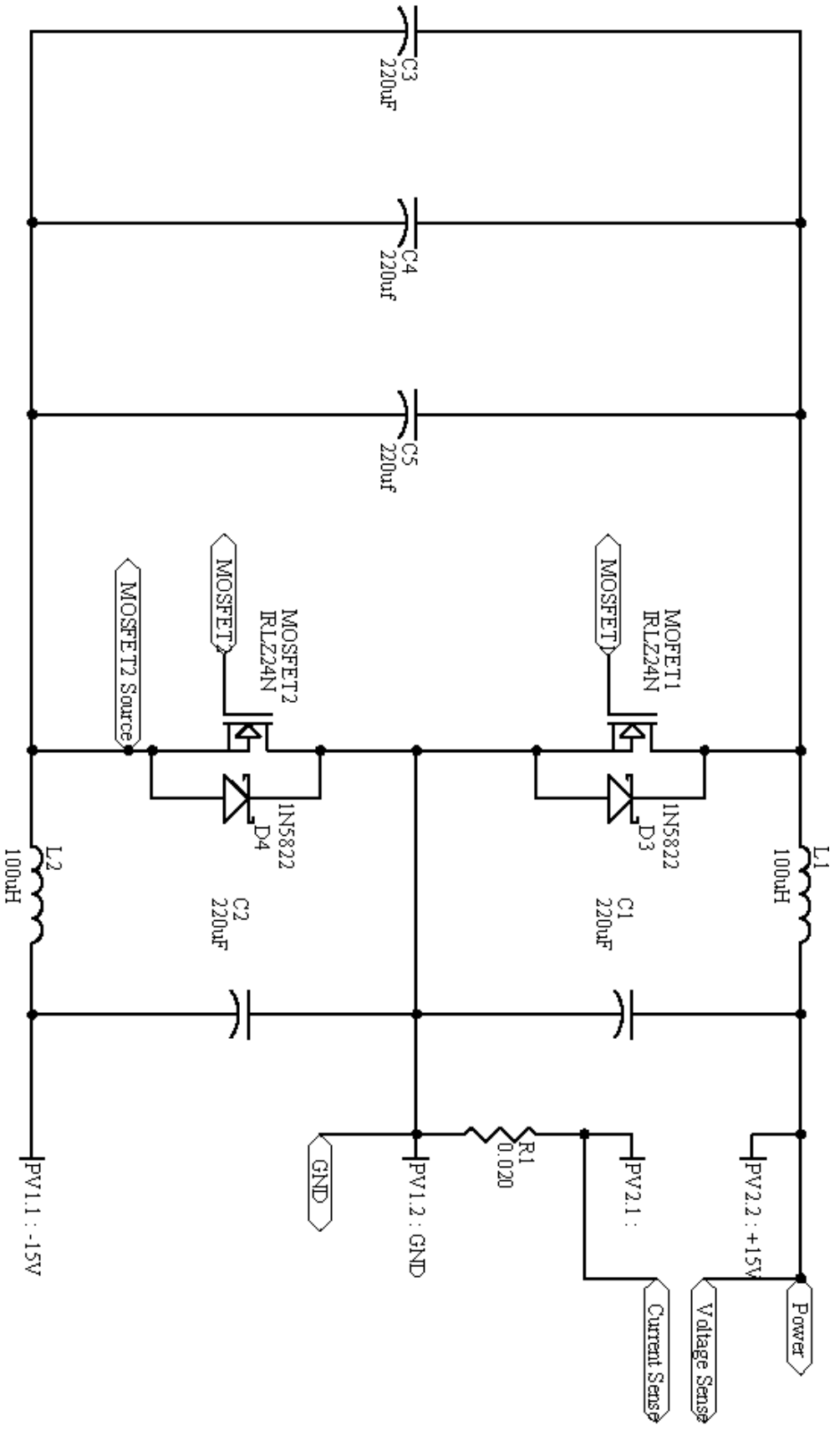


Figure D.4 - Cuk Converter

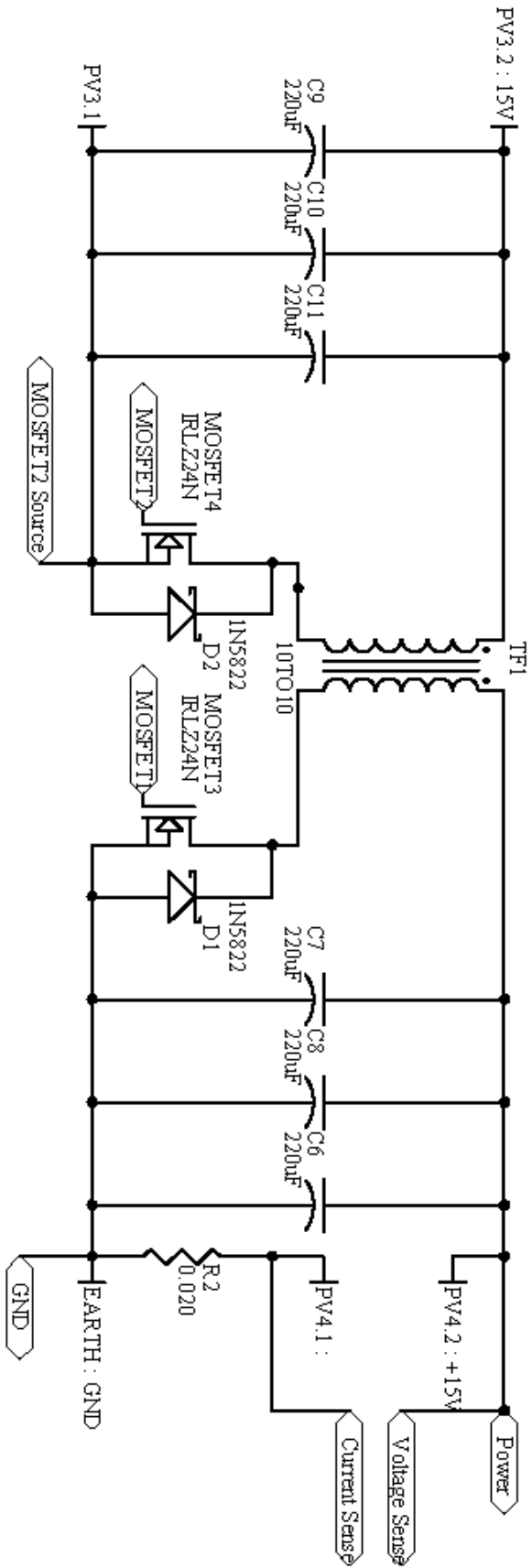


Figure D.5 - Flyback Converter



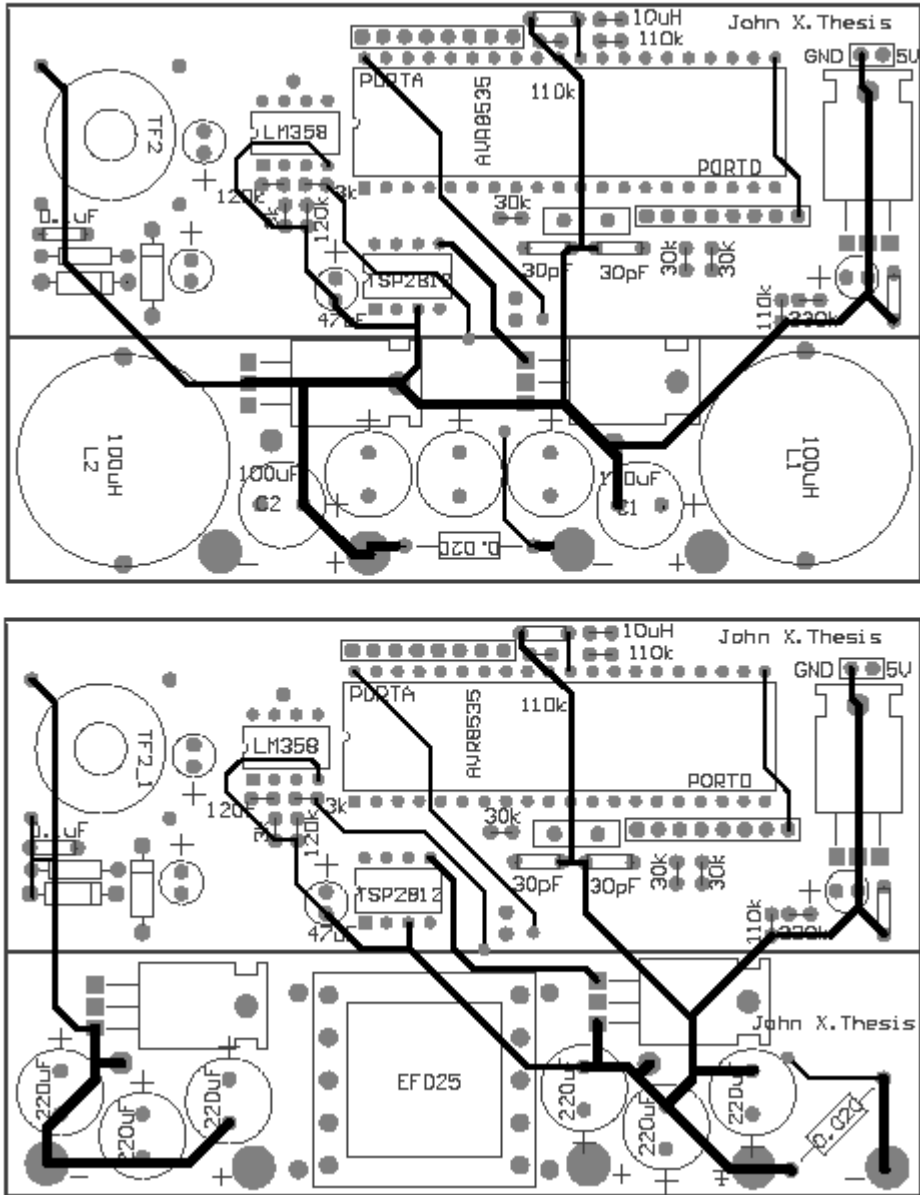


Figure E.2 - Bottom layer PCB, Cuk (top), Flyback (bottom)

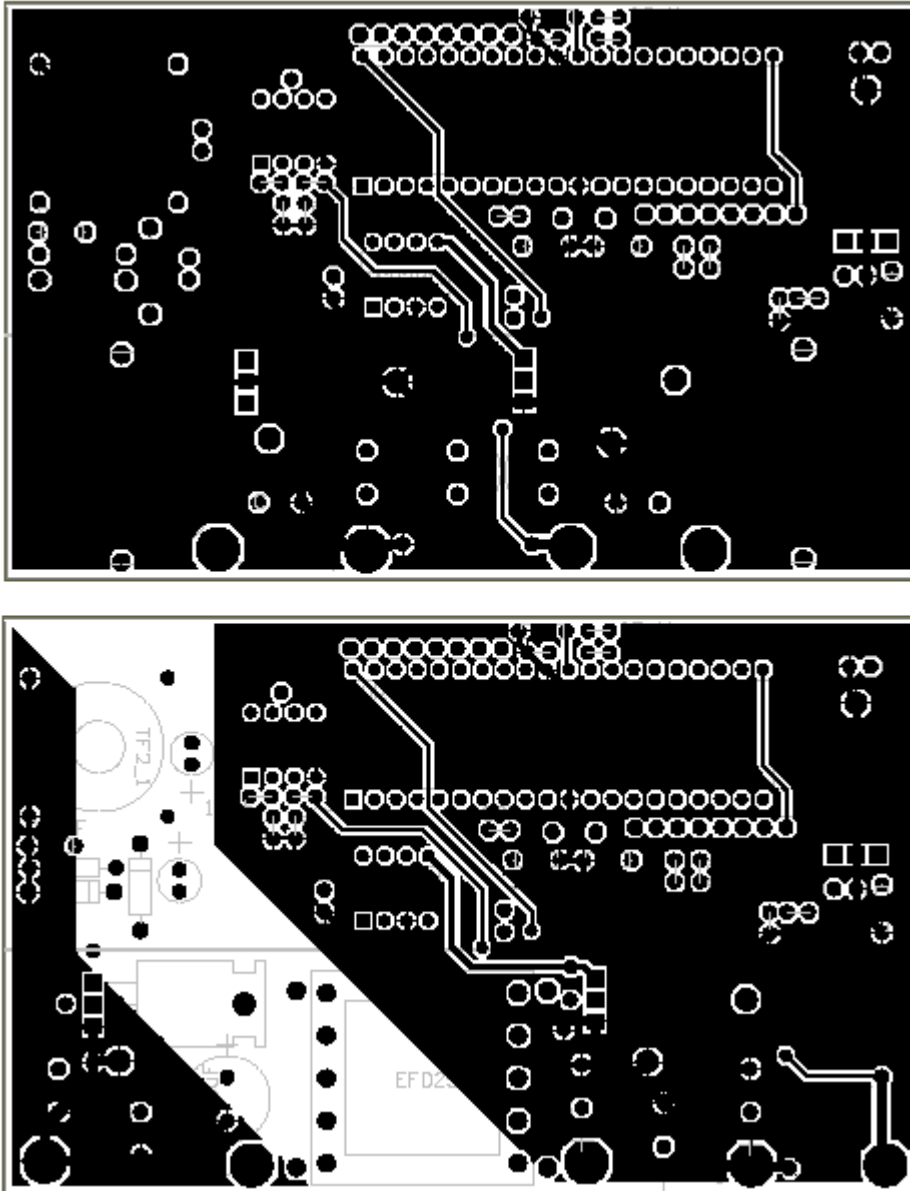


Figure E.3 - Bottomlayer PCB with ground plane, Cuk (top), Flyback (bottom)

# Appendix F - Microcontroller Code

## C Code for Perturb and Observe

```
----- START MPPT.c -----
/* Author: John Xue
 *
 * Description: AT90S8535 converter switching code
 *           Outputs PWM to pins 18 and 19, at 100kHz.
 *           Maximum power point tracking using Perturb and Observe method
 *
 * References: Inline assembly coding structure obtained from
 *           GCC AVR Inline Assembler Codebook Version 1.6 [42]
 *
 * Date: 18/9/02
 */

/* Values in kHz */
#include <io.h>
#include <interrupt.h>
#include <sig-avr.h>

#define CLOCK                8000
#define FREQ                  100

/*
 * To achieve fast switching this code must be compiled into assembly
 * then the extra pushing and popping of registers should be deleted.
 * At 100kHz there are 80 clock cycles available for a 8Mhz crystal.
 * The below code uses,
 * 4 clock cycles to jump to the ISR,
 * 4 clock cycles for the cbi and sbi combined,
 * and 4 clock cycles for the reti (return from subroutine).
 *
 * These ISRs fire once each so there is a total of 12*2 = 24 clock cycles
 * used to generate the modulation. That is 30% of the CPU used on switching.
 */

SIGNAL (SIG_OUTPUT_COMPARE1A)// Compare interrupt routine
{
    cbi (PORTD,4);
    sbi (PORTD,5);
}

SIGNAL (SIG_OUTPUT_COMPARE1B)// Compare interrupt routine
{
    cbi (PORTD,5);
```

```

        sbi (PORTD,4);
    }

    /*
    * delay negative to transfer more power to isolated side
    * delay positive to transfer more power to non-isolated side
    */
    int main( void )
    {
        unsigned char vshsb,vslsb;
        unsigned char delay;
        unsigned int ADCVsense, ADCCsense;
        unsigned int LastP, LastP2;
        unsigned char ADCSR_data,ADCH_data,ADCL_data,i; // ADC Register Variables
        unsigned char AVG_Number;
        unsigned delay_change;

        outp(0xF2, DDRD); /* define PORTD as Inputs and outputs */

        // turn switches off
        cbi (PORTD,4);
        cbi (PORTD,5);

        outp(0xFF, DDRB); /* define PORTB as Output (Leds)*/
        outp(0x00, DDRA); /* define PORTA as Inputs*/

        delay = (CLOCK/FREQ)/2-1; /* default of timer1 high byte 50% */

        /* Switches PB3,PB4 for Interrupt 0 and 1 */
        //outp((1 << INT0) | (1 << INT1), GIMSK);

        outp((1 << ISC01) | (1 << ISC10) | (1 << ISC11), MCUCR);

        /* Timer Interrupts */
        outp( (1 << OCIE1A) | (1 << OCIE1B), TIMSK);

        outp(0, TCNT1H); /* Init T1 */
        outp(0, TCNT1L);

        outp(0x00, OCR1BH); /* Compare value of T1 */
        outp(delay, OCR1BL);

        outp(0x00, OCR1AH); /* Compare value of T1 */
        outp((CLOCK/FREQ), OCR1AL);
        outp(0, TCCR1A); /* Timer mode with no output */

```

```

outp( 1 | 0x08 , TCCR1B); /* counting with ck and reset timer on compareA */

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;

// ADC initialization
// ADC Clock frequency: 62.500 kHz
ADCSR=0x87;

LastP = 0;
LastP2 = 0;
delay_change = 1;
AVG_Number = 25;

sei();

for (;;) {

    ADCVsense = 0;                // Initialise this variable to zero.
    ADCCsense = 0;                // Initialise this variable to zero.
    for(i=0;i<AVG_Number;i++)    // Were taking the average AVG_Number samples.
    {
        //get from pin A0
        outp(0,ADMUX);
        // Start a conversion
        outp((BV(ADEN)|BV(ADSC))0x07,ADCSR);
        // Get the ADC Value
        do ADCSR_data = inp(ADCSR); while( (BV(ADIF) & ADCSR_data) != 0x10);
        // Clear the ADC conv interrupt bit
        outp(BV(ADIF)|ADCSR_data,ADCSR);
        // Read the Low Byte
        ADCL_data= inp(ADCL);
        // Read the High Byte
        ADCH_data= inp(ADCH);
        // Convert the two 8-bit bytes into a 16 bit word
        ADCVsense = ((ADCH_data * 0x100) + ADCL_data) + ADCVsense;

        //get from pin A1
        outp(1,ADMUX);
        outp((BV(ADEN)|BV(ADSC))0x07,ADCSR);
        do ADCSR_data = inp(ADCSR); while( (BV(ADIF) & ADCSR_data) != 0x10);
        outp(BV(ADIF)|ADCSR_data,ADCSR);
        ADCL_data= inp(ADCL);
        ADCH_data= inp(ADCH);
    }
}

```

```

        ADCCsense = ((ADCH_data * 0x100) + ADCL_data) + ADCCsense;
    }

    // We are taking the average of AVG_Number samples.
    ADCCsense = ADCCsense / AVG_Number;
    ADCVsense = ADCVsense / AVG_Number;

    //round by four
    ADCCsense = ADCCsense / 4;
    ADCVsense = ADCVsense / 4;

    LastP2 = LastP;
    LastP = ADCCsense * ADCVsense;

    /*
    * If going in correct direction, keep going
    */

    if (LastP > LastP2)
    {
        sbi (PORTB,1);
        if (delay_change == 1)
        {
            delay = delay + 1;
            sbi (PORTB,2);
        }
        else
        {
            delay = delay - 1;
            cbi (PORTB,2);
        }
    }
    /*
    * If going in wrong direction, change direction
    */
    if (LastP < LastP2)
    {
        cbi (PORTB,1);
        if (delay_change == 1)
        {
            delay_change = 0;
            delay = delay - 1;
            cbi (PORTB,2);
        }
        else
        {
            delay_change = 1;

```

```

        delay = delay + 1;
        sbi (PORTB,2);
    }
}
if (delay < 30)
    delay = 30;

if (delay > 50)
    delay = 50;

outp(delay, OCR1BL);
}
}
----- ENDS MPPT.c -----

```

## C Code Voltage Regulation

```

----- START MPPT.c -----
/* Author: John Xue
 *
 * Description: AT90S8535 converter switching code
 *             Outputs PWM to pins 18 and 19, at 100kHz
 *             Regulates the output to a specific voltage (12V)
 *
 *
 * Date: 18/9/02
 */

/* Values in kHz */
#include <io.h>
#include <interrupt.h>
#include <sig-avr.h>

#define CLOCK          8000
#define FREQ           100

/*
 * To achieve fast switching this code must be compiled into assembly
 * then the extra pushing and popping of registers should be deleted.
 * At 100kHz there are 80 clock cycles available for a 8Mhz crystal.
 * The below code uses,
 * 4 clock cycles to jump to the ISR,
 * 4 clock cycles for the cbi and sbi combined,
 * and 4 clock cycles for the reti (return from subroutine).
 *
 * These ISRs fire once each so there is a total of 12*2 = 24 clock cycles
 * used to generate the modulation. That is 30% of the CPU used on switching.
 */

SIGNAL (SIG_OUTPUT_COMPARE1A) // Compare interrupt routine
{
    cbi (PORTD,4);
    sbi (PORTD,5);
}

SIGNAL (SIG_OUTPUT_COMPARE1B) // Compare interrupt routine
{
    cbi (PORTD,5);
    sbi (PORTD,4);
}

```

```

}

unsigned int GetADCCConversionAVG (unsigned char AVG_Number)
{
    unsigned char ADCSR_data,ADCH_data,ADCL_data,i; // ADC Register Variables
    unsigned int ADC_16; // Variable that holds 16 bit ADC Value
    ADC_16 = 0; // Initialise this variable to zero.
    for(i=0;i<AVG_Number;i++) // Were taking the average AVG_Number samples.
    {
        // Start a conversion
        outp((BV(ADEN)|BV(ADSC)|0x07),ADCSR);
        // Get the ADC Value
        do ADCSR_data = inp(ADCSR); while( (BV(ADIF) & ADCSR_data) != 0x10);
        // Clear the ADC conv interrupt bit
        outp(BV(ADIF)|ADCSR_data,ADCSR);
        // Read the Low Byte
        ADCL_data= inp(ADCL);
        // Read the High Byte
        ADCH_data= inp(ADCH);
        // Convert the two 8-bit bytes into a 16 bit word
        ADC_16 = ((ADCH_data * 0x100) + ADCL_data) + ADC_16;
    }
    // We are taking the average of AVG_Number samples.
    ADC_16 = ADC_16 / AVG_Number;
    // Return the 16-Bit Word
    return(ADC_16);
}

```

```

/*
 * delay negative to transfer more power to isolated side
 * delay positive to transfer more power to non-isolated side
 */
int main( void )
{
    unsigned char vshb,vslsb;
    unsigned char delay;
    unsigned int ADCreturn;
    outp(0xF2, DDRD); /* define PORTD as Inputs and outputs */

    // turn switches off
    cbi (PORTD,4);
    cbi (PORTD,5);

    outp(0xFF, DDRB); /* define PORTB as Output (Leds)*/
    outp(0x00, DDRA); /* define PORTA as Inputs*/

    delay = (CLOCK/FREQ)/2-1; /* default of timer1 high byte 50% */

    /* Switches PB3,PB4 for Interrupt 0 and 1 */
    //outp((1 << INT0) | (1 << INT1), GIMSK);

    outp((1 << ISC01) | (1 << ISC10) | (1 << ISC11), MCUCR);

    /* Timer Interrupts */
    outp( (1 << OCIE1A) | (1 << OCIE1B), TIMSK);

    outp(0, TCNT1H); /* Init T1 */
    outp(0, TCNT1L);

    outp(0x00, OCR1BH); /* Compare value of T1 */
    outp(delay, OCR1BL);

    outp(0x00, OCR1AH); /* Compare value of T1 */
    outp((CLOCK/FREQ), OCR1AL);
    outp(0, TCCR1A); /* Timer mode with no output */
    outp( 1 | 0x08 , TCCR1B); /* counting with ck and reset timer on compareA */
}

```

```

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;

// ADC initialization
// ADC Clock frequency: 62.500 kHz
ADCSR=0x87;

sei();

for (;;) {
    // every 50 of ADCreturn is 1V.

    outp(0,ADMUX); //get from pin A0
    ADCreturn = GetADConversionAVG(50);
    outp((ADCreturn & 0xFF), PORTB);

    if (ADCreturn > 600 && delay > 30)
        delay = delay - 1;

    if (ADCreturn < 600 && delay < 50)
        delay = delay + 1;

    outp(delay, OCR1BL);
    //outp(PORTB, vs1sb);
}
}
----- ENDS MPPT.c -----

```

## Assembly Code for Converter Switching

Look for the following lines of code in the original assembly file.

```

----- START Original File -----
.LM1:
/* prologue: frame size=0 */
    push __zero_reg__
    push __tmp_reg__
    in __tmp_reg__, __SREG__
    push __tmp_reg__
    clr __zero_reg__
/* prologue end (size=5) */
    .stabs 68,0,36,.LM2-__vector_6
.LM2:
    cbi 50-0x20,4
    .stabs 68,0,37,.LM3-__vector_6
.LM3:
    sbi 50-0x20,5
    .stabs 68,0,38,.LM4-__vector_6
.LM4:
/* epilogue: frame size=0 */
    pop __tmp_reg__
    out __SREG__, __tmp_reg__
    pop __tmp_reg__
    pop __zero_reg__
    reti
/* epilogue end (size=5) */
/* function __vector_6 size 12 (2) */
.Lfe1:
    .size __vector_6,.Lfe1-__vector_6
.Lscope0:
    .stabs "",36,0,0,.Lscope0-__vector_6
    .stabs "__vector_7:F(0,20)",36,0,41,__vector_7

```

```

.global    __vector_7
__vector_7:
.type     __vector_7,@function
__vector_7:
.stabn 68,0,41,,LM5-__vector_7
.LM5:
/* prologue: frame size=0 */
push __zero_reg__
push __tmp_reg__
in __tmp_reg__, __SREG__
push __tmp_reg__
clr __zero_reg__
/* prologue end (size=5) */
.stabn 68,0,42,,LM6-__vector_7
.LM6:
cbi 50-0x20,5
.stabn 68,0,43,,LM7-__vector_7
.LM7:
sbi 50-0x20,4
.stabn 68,0,44,,LM8-__vector_7
.LM8:
/* epilogue: frame size=0 */
pop __tmp_reg__
out __SREG__, __tmp_reg__
pop __tmp_reg__
pop __zero_reg__
reti
/* epilogue end (size=5) */
/* function __vector_7 size 12 (2) */
.Lfe2:

```

-----END Original File-----

Remove the popping and pushing of registers as shown below.

-----START Adjusted File-----

```

.LM1:
cbi 50-0x20,4
sbi 50-0x20,5
reti
/* epilogue end (size=5) */
/* function __vector_6 size 12 (2) */
.Lfe1:
.size    __vector_6,.Lfe1-__vector_6
.Lscope0:
.stabs   "" ,36,0,0,.Lscope0-__vector_6
.stabs   "__vector_7:F(0,20)",36,0,41,__vector_7
.global  __vector_7
__vector_7:
.type     __vector_7,@function
__vector_7:
.stabn 68,0,41,,LM5-__vector_7
.LM5:
cbi 50-0x20,5
sbi 50-0x20,4
reti
/* epilogue end (size=5) */
/* function __vector_7 size 12 (2) */
.Lfe2:

```

-----END Adjusted File-----

# Appendix G - PSpice Simulation Circuits

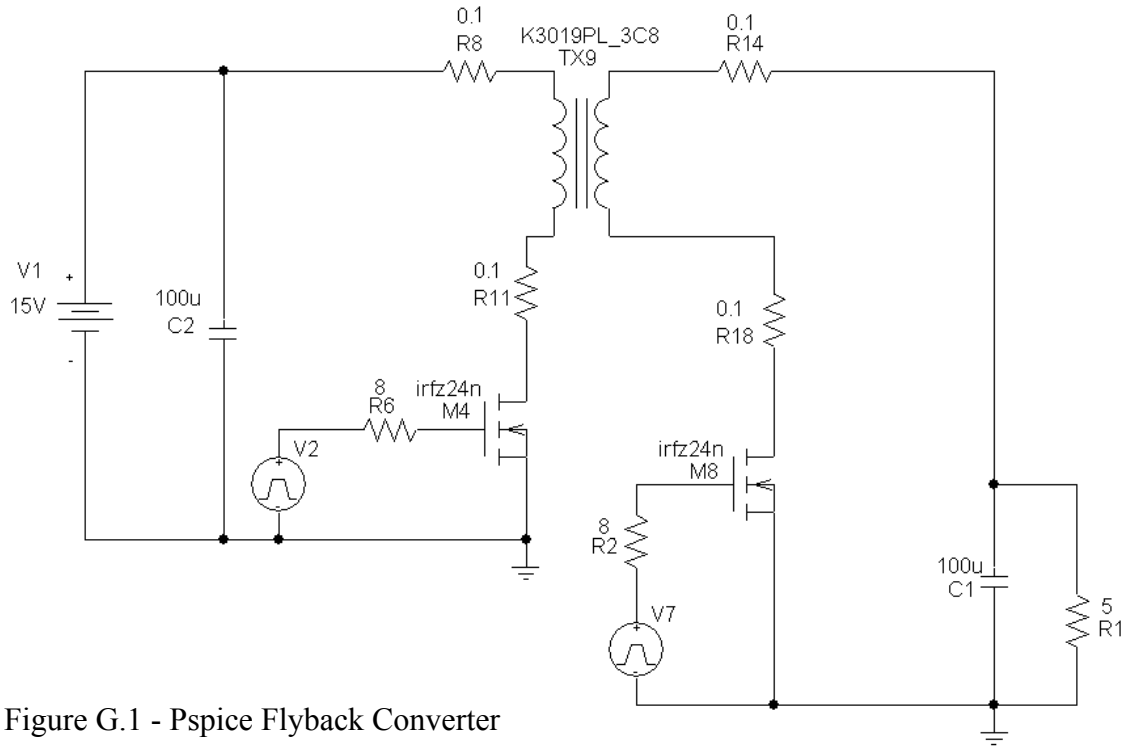


Figure G.1 - Pspice Flyback Converter

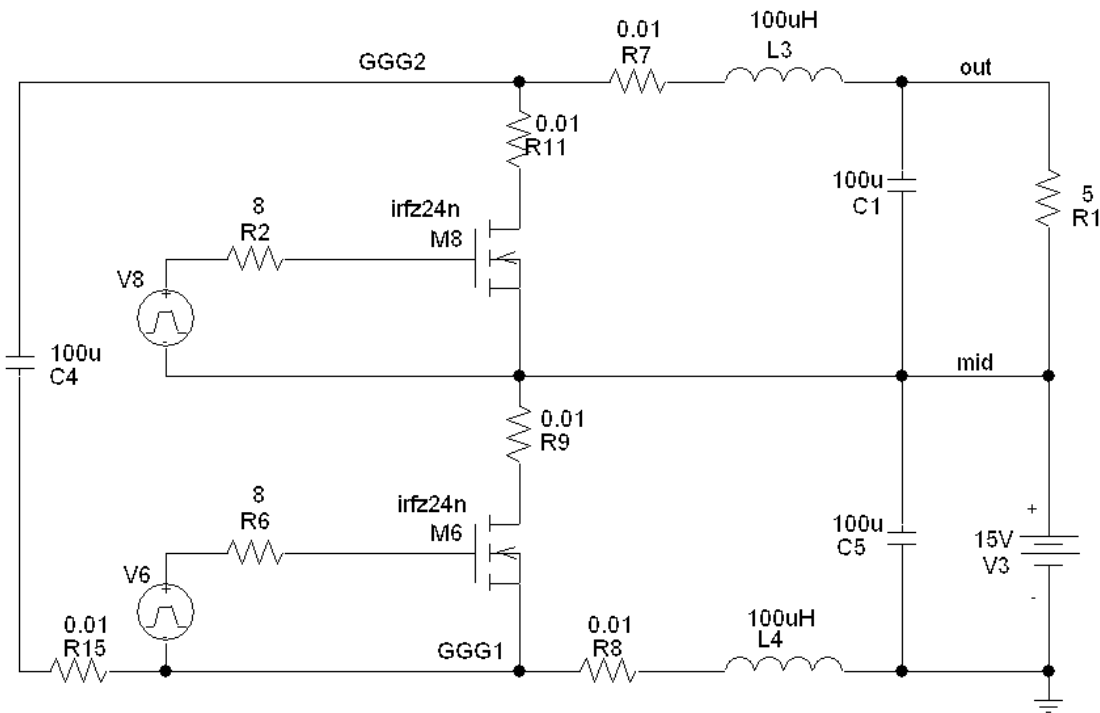


Figure G.2 - Pspice Cuk Converter

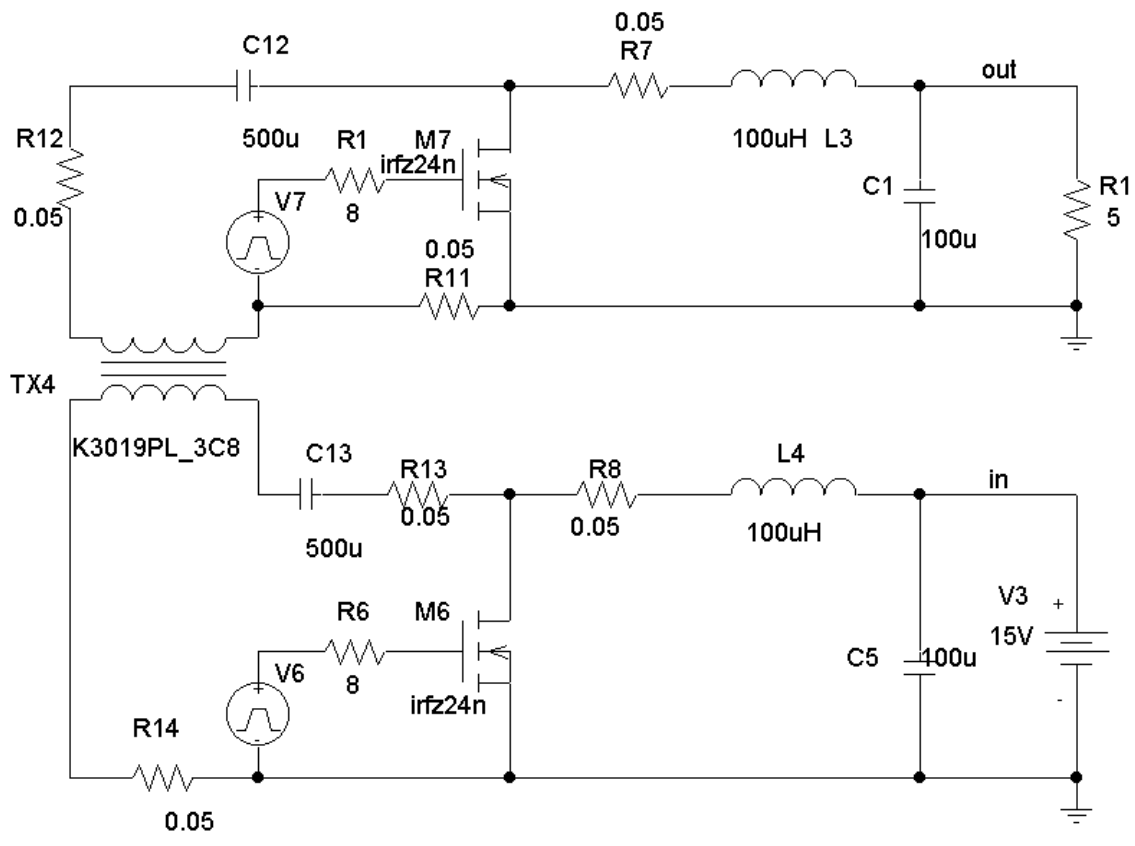


Figure G.3 - Isolated Cuk Converter

## Appendix H - PSpice Simulation Raw Results

Table H.1 - Cuk Converter

Cuk Converter								
Variation of loads testing							Loss Analysis	
Load	Vin (V)	Vout + Vin	Vout (V)	Iin (A)	Iout (A)	Efficiency	Name	Power (W)
5	15.00	28.35	13.35	2.664	2.671	0.8924	In	46.893
6	15.00	28.48	13.48	2.261	2.246	0.8923	Out	41.501
7.5	15.00	28.60	13.60	1.828	1.814	0.8997	L3	0.357
10	15.00	28.68	13.68	1.341	1.368	0.9299	L4	0.414
15	15.00	28.64	13.64	0.949	0.909	0.8708	M6	1.284
20	15.00	28.71	13.71	0.708	0.685	0.8839	M8	2.568
30	15.00	29.59	14.59	0.669	0.486	0.7071	Resistors	0.768
45.7	15.00	33.08	18.08	0.433	0.396	1.1025		
50	15.00	33.84	18.84	0.439	0.377	1.0800		
75	15.00	36.78	21.78	0.467	0.290	0.9031		
150	15.00	40.19	25.19	0.551	0.168	0.5118		
200	15.00	41.23	26.23	0.587	0.131	0.3907		
Frequency Variation								
Frequency (Hz)	Vin (V)	Vout + Vin	Vout (V)	Iin (A)	Iout (A)	Efficiency		
50k	15.00	27.96	12.96	2.527	2.592	0.8862		
100k	15.00	28.35	13.35	2.664	2.671	0.8924		
200k	15.00	29.18	14.18	3.018	2.835	0.8877		

Table H.2 - Synchronously Switched Cuk Converter

Cuk Converter With Synchronous Rectification							
Variation of loads testing							
Load	Vin (V)	Vout + Vin	Vout (V)	Iin (A)	Iout (A)	Efficiency	
5	15.00	28.89	13.89	2.746	2.779	0.9371	
6	15.00	29.01	14.01	2.313	2.336	0.9434	
7.5	15.00	29.11	14.11	1.875	1.887	0.9468	
10	15.00	29.30	14.30	1.430	1.430	0.9533	
15	15.00	29.46	14.46	0.984	0.964	0.9442	
20	15.00	29.54	14.54	0.771	0.727	0.9145	
30	15.00	29.67	14.67	0.532	0.489	0.8991	
45.7	15.00	29.76	14.76	0.384	0.323	0.8275	
50	15.00	29.79	14.79	0.364	0.296	0.8018	
75	15.00	29.95	14.95	0.305	0.199	0.6509	
150	15.00	30.05	15.05	0.249	0.100	0.4038	
200	15.00	30.07	15.07	0.239	0.075	0.3167	
Frequency Variation							
Frequency (Hz)	Vin (V)	Vout + Vin	Vout (V)	Iin (A)	Iout (A)	Efficiency	
50k	15.00	28.52	13.52	2.614	2.704	0.9328	
100k	15.00	28.89	13.89	2.746	2.779	0.9371	
200k	15.00	29.02	14.02	2.890	2.800	0.9056	

Table H.3 - Isolated Cuk Converter

Isolated Cuk Converter						Loss Analysis	
Variation of loads testing						Name	Power (W)
Load (ohms)	Vin (V)	Vout (V)	Iin (A)	Iout (A)	Efficiency		
5	15.00	13.77	2.954	2.753	0.8553	In	47.550
7.5	15.00	14.15	2.330	1.887	0.7640	Out	41.265
10	15.00	14.46	1.551	1.446	0.8985		
15	15.00	14.81	1.114	0.987	0.8747	L3	0.338
20	15.00	15.00	0.997	0.750	0.7524	L4	0.501
30	15.00	16.21	0.686	0.550	0.8665	M6	1.432
50	15.00	18.12	0.570	0.368	0.7792	M7	1.092
75	15.00	19.43	0.689	0.259	0.4873		
150	15.00	20.30	0.704	0.138	0.2644	Resistors	2.922
200	15.00	20.55	0.705	0.105	0.2030		
Frequency Variation							
Frequency (Hz)	Vin (V)	Vout (V)	Iin (A)	Iout (A)	Efficiency		
50k	15.00	13.35	2.778	2.669	0.8550		
100k	15.00	13.77	2.954	2.753	0.8553		
200k	15.00	14.51	3.323	2.902	0.8449		

Table H.4 - Flyback Converter

Flyback Converter						Loss Analysis	
Variation of loads testing						Name	Power (W)
Load (ohms)	Vin (V)	Vout (V)	Iin (A)	Iout (A)	Efficiency		
5	15.00	11.96	3.384	2.392	0.5636	In	51.100
7.5	15.00	12.63	2.388	1.684	0.5938	Out	28.713
10	15.00	13.00	1.850	1.300	0.6090		
15	15.00	13.39	1.280	0.893	0.6224	M4	1.201
20	15.00	13.60	0.983	0.680	0.6271	M8	2.902
30	15.00	13.81	0.677	0.460	0.6265		
45.7	15.00	13.97	0.462	0.306	0.6166	Resistors	18.284
50	15.00	13.99	0.425	0.280	0.6145		
75	15.00	14.09	0.297	0.188	0.5944		
150	15.00	14.20	0.167	0.095	0.5353		
200	15.00	14.23	0.135	0.071	0.4998		
Frequency Variation							
Frequency (Hz)	Vin (V)	Vout (V)	Iin (A)	Iout (A)	Efficiency		
50k	15.00	11.99	3.419	2.397	0.5602		
100k	15.00	11.96	3.384	2.392	0.5636		
200k	15.00	12.04	3.327	2.409	0.5812		

## Appendix I - Differential Amp Measurements

$V_{\text{sense}}$ (mV)	$V_{\text{amp}}$ (mV)	$I_{\text{cal}}$ (mA)	Amp Gain
4.8	310	240	64.58
10	540	500	54.00
15	680	750	45.33
20	850	1000	42.50
25	1050	1250	42.00
30	1250	1500	41.67
35	1460	1750	41.71
40	1660	2000	41.50
45	1900	2250	42.22
50	2120	2500	42.40
55	2320	2750	42.18
60	2360	3000	39.33
65	2560	3250	39.38
70	2760	3500	39.43
75	2960	3750	39.47
80	3120	4000	39.00
85	3350	4250	39.41
90	3540	4500	39.33
95	3710	4750	39.05
100	3710	5000	37.10
105	3710	5250	35.33

## Appendix J - 2<sup>nd</sup> Prototype Results

Table J.1 - Diode Rectified Cuk Results

Vin	Iin	Vout	Iout	Pin	Pout	Efficiency
15.00	0.321	18.42	0.109	4.82	2.01	0.417
15.00	0.312	17.13	0.130	4.68	2.23	0.476
15.00	0.309	16.37	0.150	4.64	2.46	0.530
15.00	0.308	15.68	0.170	4.62	2.67	0.577
15.00	0.306	15.04	0.190	4.59	2.86	0.623
15.00	0.310	15.02	0.204	4.65	3.06	0.659
15.00	0.310	14.63	0.220	4.65	3.22	0.692
15.00	0.338	14.98	0.242	5.07	3.63	0.715
15.00	0.348	14.77	0.260	5.22	3.84	0.736
15.00	0.360	14.59	0.270	5.40	3.94	0.730
15.00	0.427	15.34	0.323	6.41	4.95	0.774
15.00	0.444	15.22	0.341	6.66	5.19	0.779
15.00	0.466	15.07	0.360	6.99	5.43	0.776
15.00	0.499	14.90	0.399	7.49	5.95	0.794
15.00	0.540	14.76	0.437	8.10	6.45	0.796
15.00	0.579	14.68	0.474	8.69	6.96	0.801
15.00	0.638	14.59	0.530	9.57	7.73	0.808
15.00	0.736	15.21	0.591	11.04	8.99	0.814
15.00	0.793	15.11	0.645	11.90	9.75	0.819
15.00	0.868	14.99	0.711	13.02	10.66	0.819
15.00	0.981	14.65	0.813	14.72	11.91	0.809
15.00	1.163	14.97	0.940	17.45	14.07	0.807
15.00	1.478	15.36	1.100	22.17	16.90	0.762
14.85	1.563	15.22	1.086	23.21	16.53	0.712

Table J.2 - Synchronous Rectified Cuk Results

Vin	Iin	Vout	Iout	Pin	Pout	Efficiency
15.01	0.13	14.35	0.061	1.98	0.88	0.442
15.13	0.15	14.53	0.080	2.27	1.16	0.512
15.13	0.17	14.52	0.100	2.57	1.45	0.565
15.13	0.19	14.50	0.120	2.87	1.74	0.605
15.13	0.21	14.48	0.140	3.18	2.03	0.638
15.12	0.23	14.46	0.160	3.48	2.31	0.665
15.12	0.25	14.44	0.180	3.78	2.60	0.688
15.12	0.28	14.40	0.220	4.23	3.17	0.748
15.11	0.31	14.40	0.250	4.68	3.60	0.769
15.11	0.39	14.22	0.333	5.89	4.74	0.804
15.10	0.40	14.18	0.345	6.04	4.89	0.810
15.10	0.44	13.92	0.393	6.64	5.47	0.823
15.10	0.46	13.30	0.437	6.95	5.81	0.837
15.10	0.48	13.14	0.456	7.25	5.99	0.827
15.10	0.51	13.11	0.477	7.70	6.25	0.812
15.09	0.57	13.07	0.543	8.60	7.10	0.825
15.08	0.60	13.03	0.585	9.05	7.62	0.842
15.07	0.72	12.98	0.714	10.85	9.27	0.854
15.07	0.81	12.92	0.828	12.21	10.70	0.876
15.06	0.87	12.89	0.888	13.10	11.45	0.874
15.05	0.94	12.84	0.968	14.15	12.43	0.879
15.05	1.01	12.80	1.040	15.20	13.31	0.876
15.04	1.07	12.80	1.120	16.09	14.34	0.891
15.03	1.18	12.70	1.238	17.74	15.72	0.887
15.02	1.33	12.61	1.398	19.98	17.63	0.882
15.01	1.35	12.59	1.412	20.26	17.78	0.877
15.01	1.39	12.56	1.468	20.86	18.44	0.884
14.99	1.57	12.45	1.665	23.53	20.73	0.881

Table J.3 - Cuk Diode Rectified With Schottky diodes Removed

Vin	lin	Vout	Iout	Pin	Pout	Efficiency
14.7	0.27	14.81	0.060	3.969	0.889	0.224
14.7	0.29	14.66	0.101	4.263	1.481	0.347
14.7	0.32	14.52	0.161	4.704	2.338	0.497
14.7	0.34	14.46	0.200	4.998	2.892	0.579
14.7	0.35	14.43	0.223	5.145	3.218	0.625
14.7	0.37	14.34	0.271	5.439	3.886	0.714
14.7	0.38	14.31	0.291	5.586	4.164	0.745
14.7	0.40	14.25	0.322	5.880	4.589	0.780
14.7	0.44	14.14	0.369	6.468	5.218	0.807
14.7	0.47	14.06	0.405	6.909	5.694	0.824
14.7	0.58	13.95	0.512	8.526	7.142	0.838
14.7	0.68	13.90	0.608	9.996	8.451	0.845
14.7	0.93	13.83	0.694	13.671	9.598	0.702

Table J.4 - Cuk Synchronous Rectified With Schottky Diodes Removed

Vin	lin	Vout	Iout	Pin	Pout	Efficiency
14.7	0.12	14.15	0.053	1.764	0.750	0.425
14.7	0.13	14.14	0.066	1.911	0.933	0.488
14.7	0.16	14.12	0.100	2.352	1.412	0.600
14.7	0.20	14.10	0.140	2.940	1.974	0.671
14.7	0.22	14.09	0.154	3.234	2.170	0.671
14.7	0.27	14.09	0.208	3.969	2.931	0.738
14.7	0.33	14.06	0.277	4.851	3.895	0.803
14.7	0.38	14.00	0.320	5.586	4.480	0.802
14.7	0.44	13.93	0.402	6.468	5.600	0.866
14.7	0.53	13.48	0.500	7.791	6.740	0.865
14.7	0.55	12.74	0.530	8.085	6.752	0.835
14.7	0.62	12.74	0.599	9.114	7.631	0.837
14.7	0.71	12.69	0.704	10.437	8.934	0.856
14.7	0.80	12.65	0.805	11.760	10.183	0.866
14.7	0.89	12.63	0.901	13.083	11.380	0.870
14.7	1.05	12.49	1.070	15.435	13.364	0.866
14.7	1.12	12.45	1.150	16.464	14.318	0.870
14.7	1.25	12.38	1.300	18.375	16.094	0.876
14.7	1.34	12.33	1.368	19.698	16.867	0.856
14.7	1.41	12.33	1.460	20.727	18.002	0.869
14.7	1.61	12.19	1.660	23.667	20.235	0.855

Table J.5 - Flyback synchronous rectification

Vin	lin	Vout	Iout	Pin	Pout	Efficiency
15.00	14.25	0.146	0.28	4.125	2.081	0.504
15.00	14.25	0.181	0.31	4.65	2.579	0.555
15.00	14.20	0.300	0.42	6.3	4.260	0.676
15.00	14.15	0.438	0.54	8.1	6.198	0.765
15.00	14.15	0.452	0.54	8.1	6.396	0.790
15.00	14.15	0.490	0.59	8.85	6.934	0.783
15.00	14.00	0.609	0.70	10.5	8.526	0.812
14.95	13.48	0.706	0.77	11.5115	9.517	0.827
14.95	12.83	0.802	0.86	12.78225	10.290	0.805
14.95	12.75	0.936	0.98	14.651	11.934	0.815
14.95	12.75	1.010	1.04	15.548	12.878	0.828
14.95	12.68	1.110	1.14	17.043	14.075	0.826
14.95	12.60	1.260	1.27	18.9865	15.876	0.836
14.95	12.58	1.310	1.33	19.8835	16.480	0.829
14.95	12.50	1.411	1.42	21.229	17.638	0.831
14.95	12.44	1.590	1.58	23.621	19.780	0.837
14.98	11.53	3.371	3.10	46.438	38.868	0.837